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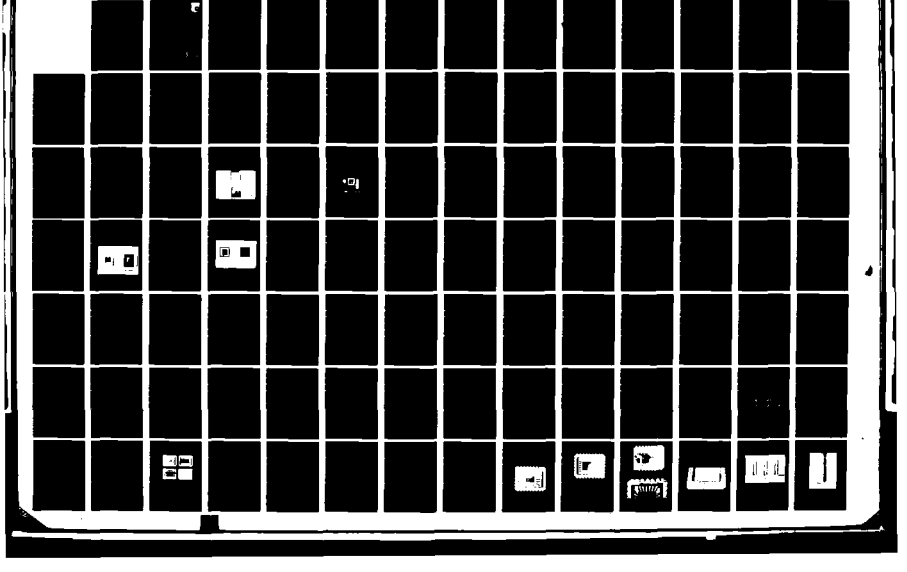

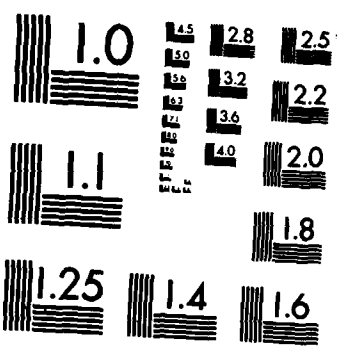

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LEADLESS CHIP CARRIER PACKAGING AND CAD/CAM-SUPPORTED WIRE WRAP INTERCONNECT TECHNOLOGY FOR SUBNANOSECOND ECL

Mayo Clinic/Mayo Foundation
Special Purpose Processor Development Group
Department of Physiology/Biophysics
Rochester, Minnesota 55905

DECEMBER 1982

Interim Report for Period July 1, 1981 through June 30, 1982

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This technical report has been reviewed and is approved for publication.

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Subnanosecond ECL	Gallium Arsenide Digital Logic

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This document is the third year interim report for a four-year program to refine and develop Computer-Aided Design protocols for implementation of subnanosecond Emitter Coupled Logic in High-Speed Computer Modules using a wire wrap interconnection medium. The software and user manual for implementation guides are not part of the actual report.

This report describes the results of work conducted in the third year

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20. ABSTRACT (Continued)

of a four year program to develop rapid methods for designing and prototyping high-speed digital processor systems using subnanosecond emitter coupled logic (ECL). The third year effort was divided into two separate sets of tasks. In Task 1, described in Sections III-VII of this report, we have nearly completed development of new sets of design rules, interconnection protocols, special components, and logic panels, for a technology based upon specially designed leadless ceramic chip carriers developed at Mayo Foundation. Task 2, described in Sections VIII and IX of this report, continued the development of a comprehensive computer-aided design/computer-aided manufacturing (CAD/CAM) software package which is specifically tailored to support the peculiar design requirements of processors operating in a high clock rate, transmission line environment, either with subnanosecond ECL components or with any other families of subnanosecond devices. The CAD/CAM software package has been structured to be sufficiently flexible to assimilate advances in device and component technology, e.g., Gallium Arsenide digital devices, and macrocell arrays both in Silicon and in GaAs, and to accept new sets of design rules resulting from advances in engineering design practice. This CAD/CAM capability is being continually upgraded to incorporate operator-interactive design aids which will allow hierarchical block-level design extending down to and encompassing the integrated circuit level.

FOREWORD

This interim report summarizes work performed under the third year of Contract F33615-79-C-1875 from the Avionics Laboratory to develop fabrication and design protocols, appropriate components and materials, as well as computer-aided design software, to allow rapid fabrication of prototype special-purpose processors based upon high-speed subnanosecond emitter coupled logic (ECL). This work has been performed by members of the Special-Purpose Processor Development Group, Department of Physiology and Biophysics, Mayo Clinic/Mayo Foundation, Rochester, Minnesota, and has been administered by the Avionics Laboratory, Wright Patterson Air Force Base, Ohio, Mr. William A. Anderson (AFAL/AADE-3), Contract Monitor.

The report was submitted by the authors on December 1, 1982, and covers the interim report period from July 1, 1981, through June 30, 1982. The work was performed under the principal investigator, Barry K. Gilbert, Ph.D., Director of the Special-Purpose Processor Development Group, Mayo Clinic/Mayo Foundation. The following members of the Special-Purpose Processor Development Group have both participated in the performance of the work under this project, and have also assisted in the preparation of the text and figures in the body of this report:

T. M. Kinter:	Computer-Aided Design Software
D. J. Schwab:	Leadless Chip Carrier and Packaging Development; Prototype Processor Design
K. M. Rice:	Operator-Interactive CAD graphics Interface
L. M. Krueger:	Microcontroller Design, Meta-Assembler and Microcode Simulator Design
B. A. Naused:	Architectural Studies
S. V. Colvin:	Drafting, Fabrication, and Circuit Test
E. M. Doherty:	Report Preparation

Subsequent interim reports under this contract will discuss continuing efforts to improve the characteristics of LCCC encapsulation for ECL and Gallium Arsenide digital integrated circuits, and to expansions of the computer-aided design software to support the use of multilayer ceramic logic board technology and hierarchical system design.

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SECTION I

INTRODUCTION

The following material represents the results of work conducted in the third year of a project to develop techniques which allow the rapid fabrication of ultra-high throughput signal processors employing parallelism, pipelining, and high-speed digital logic. The following areas are under investigation in this effort: high-speed digital device technology; improved component packaging technology; new approaches to the fabrication of circuit boards which can support transmission-line interconnects; and design and fabrication rules which assure very high computational throughput while preserving adequate system noise margins. New prototype processors must usually be designed in a reasonable duration by a relatively small group of people, whether the project is carried out in a biomedical research environment such as that at Mayo Foundation, or within the prototype labs of large corporations. It is thus absolutely necessary that the most flexible and powerful computer aided design tools be available to improve the chances of success in such projects. Hence, this report will reflect not only our continuing evolution of hardware technology capabilities, but also our commitment to computer aided design and manufacturing tools for signal processors operating at very high clock rates.

Although traditionally we have employed high-speed silicon emitter coupled logic (ECL), the recent availability of Gallium

Arsenide (GaAs) integrated circuits at the MSI integration level has motivated us to examine these early components. Since GaAs devices exhibit gate propagation delays and wavefront risetimes 2 to 3 times faster than those of ECL, the same design constraints which we have been developing for ECL will apply to GaAs components to an even greater extent. We intend to satisfy these more demanding performance constraints, both in our design and fabrication rules, and in the sophistication of the computer aided design software used to develop GaAs-based systems. Nonetheless, we will attempt to retain a rapid design and fabrication capacity for signal processors containing several thousand integrated circuits or more.

Mayo Foundation is motivated to undertake such development tasks because of the existence of a large and expanding class of high volume computational problems arising from biomedical research. It is of interest to note that many of the largest military computational problems have analogs in the biomedical world. To illustrate the fact that biomedical problems can often be of equivalent computational complexity to those found in the military environment, we have co-opted a graph developed for the Very High-Speed Integrated Circuits (VHSIC) project, adding to that graph two examples of computational problems derived from biomedicine. The Dynamic Spatial Reconstructor (DSR), a state-of-the-art real-time volume-imaging x-ray computed tomography unit under development at Mayo Foundation, has been described extensively in the open literature. This machine is capable of

collecting sufficient data to allow the reconstruction of a volume image of the human thorax, with the data collection procedure repeated at 60-per-second repetition rates. Each volume image is composed of 240 one mm thick slabs of tissue, with each equivalent cross sectional image in turn composed of 40,000 separate pixels in a 200 x 200 array. Of perhaps additional interest, the resulting raw data downlink bandwidth of this system is 200 megabytes per second, with data collection occurring in 5-10 second bursts.

Following the approach of the now well-known "VHSIC slide" (redrawn in Figure 1), we parameterized the size of the DSR computational problem. The system clock rate necessary to achieve sufficient throughput was multiplied by the number of logic gates necessary to fabricate a system of enough power to accomplish the task; the result of this computation delineated a performance region on the graph of Figure 1.

This figure also plots the required performance of several computers designed for high throughput tasks derived from military applications. The diagonal dotted lines represent performance products over a range of 10^{11} to 10^{14} gate-Hertz, and a range of computation rates from 1 million to 50 billion arithmetic operations per second. The processing rates for the Dynamic Spatial Reconstructor (DSR) are presented at five percent of maximum data utilization, and at maximum data utilization,

both assuming 10 times longer than real time processing rates. These two performance regions thus compare in magnitude to the most complex military computational problems. Though not included in figure 1, preliminary estimates indicate that other biomedical computational tasks, such as molecular modeling and real time ultrasound-based computed tomography, are as large as or larger than the .05 data utilization DSR problem. These comparisons indicate that substantial advances in processing technology will be required to solve the most interesting biomedical and the most critical military problems.

SPEED - COMPLEXITY COMPARISON BETWEEN SELECTED BIOMEDICAL AND MILITARY COMPUTATIONAL TASKS

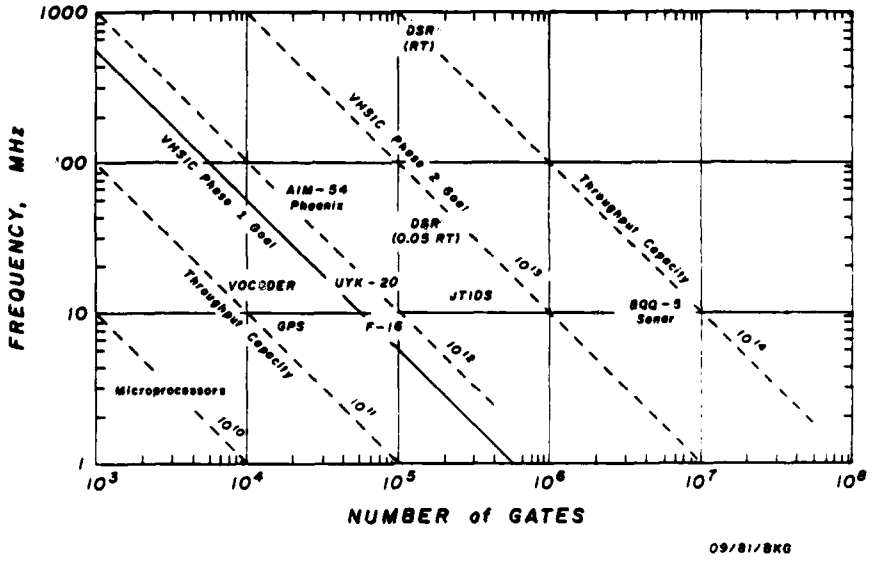


Figure 1

SECTION II

REVIEW OF YEAR TWO DATA AND EFFORTS MOTIVATED FOR YEAR THREE BY THESE RESULTS

A review of the results of the Year Two research led to the following conclusions. First, performance improvements were noted when high-speed ECL devices were packaged in leadless ceramic chip carriers and operated on a circuit board using wire wrap interconnect, in comparison to similar performance measurements made with dual inline package encapsulation; these results further confirmed that leadless ceramic chip carrier (LCCC) packaging was viable for high performance devices and should be pursued. Second, several tentative conclusions had been reached concerning the usefulness of commercially available leadless chip carriers; however, we lacked quantitative measurements of the performance characteristics of these commercial chip carriers, and hence could not confirm these conclusions. As a result, during Year Two we identified several items of electronic test equipment which would allow very accurate measurements of the parasitic reactances of flat packs, DIPs, and leadless chip carriers. Such a unit was delivered to our laboratory during the first quarter of the Year Three effort. In a later section the electrical characteristics of a variety of package formats are documented. These measurements indeed confirmed our original assumptions of the unsuitability of commercially available LCCCs, and strengthened our resolve to design a small family of these devices with improved electrical performance.

A second portion of our packaging design effort was predicated on a discovery made in July, 1981, that negated much of the development work which we had performed on a small 32-pad leadless ceramic chip carrier (which was described in the Year Two Year-End report). The size of the 32-pad LCCC had been determined through our interactions with Fairchild Camera and Instrument Corporation, i.e., by their desire to use the LCCCs resulting from this design effort as the primary encapsulation for their high-speed SSI and MSI ECL integrated circuits, and the static RAMs of the same family. Based upon the die size of integrated circuits presently available or and in development, the minimum die well dimensions, and hence external dimensions, were derived for a chip carrier for these applications; the resulting chip supported 32 contact pads on 50 ml spacing with a rectangular aspect ratio.

Thus, considerable effort was expended in the latter half of Year Two to design an appropriate 32-pad inverse-mounted LCCC and a matching logic board for the chip carrier. We had actually released both the 32-pad LCCC specification prints to Kyocera International for the manufacture of hard tooling, and also the blueprints for the design of the first multilayer logic panels to the board manufacturer, when we were notified by Fairchild Camera and Instrument Corporation that an error had been made in the calculation of the maximum die sizes which would be installed in these LCCCs; as a result we were requested to consider a redesign of the 32-pad LCCC to a 28-pad version.

We concluded that the tighter packing density which could be achieved with a 28-pad LCCC, and the improved electrical performance which would accrue from its smaller dimensions, made the redesign worth the effort. Although progress toward a compatible encapsulation and multilevel board technology for air cooled and high-power integrated circuits was temporarily retarded, the smaller carrier achieves an approximately 10-12 percent increase in board packing density. During the subsequent redesign of the multilayer logic panel, we incorporated a new design philosophy into this structure based upon insights acquired with the new impedance measurement equipment described earlier. These new board design and board fabrication philosophies will also be discussed in a later portion of the report.

Finally, our tentative conclusions from the first two years of this research regarding the importance of high quality computer aided design capabilities, and the need for attention to the transmission line interconnect nature of high-speed logic families, have been reinforced by preliminary operational results from high-speed Gallium Arsenide digital integrated circuits packaged in LCCCs and operated on conventional logic boards. These devices consistently exhibit gate delays and wavefronts 2-3 times faster than those of subnanosecond ECL. Because of the improved performance and wider signal bandwidths of the faster wavefront devices, all future developments undertaken in this

project will attempt to accomodate signal risetimes as short as 200 psec. This more stringent requirement for high performance encapsulation and board interconnect technology is an alteration in degree, not in kind, and hence can be approached by an extension of the work already under way here for high speed silicon devices.

SECTION III

IDENTIFICATION OF LEADLESS CERAMIC CHIP CARRIERS SUITABLE FOR USE IN HIGH-POWER, HIGH-FREQUENCY APPLICATIONS

Measurements of the Electrical Characteristics of Commercial Dual In-line Packages, Flat Packs, Leadless Chip Carriers, and Connectors

As discussed in the Year Two Year-End Report, the electrical characteristics of the encapsulation for high-speed integrated circuits exerts a major influence on the performance available from the integrated circuit die themselves. In general, the DC resistance of the signal leads in the encapsulation is of little consequence, since in most cases DC resistance values less than half an ohm are the rule. At high frequencies, it is the parasitic inductive and capacitive reactances of the signal leads which cause the major degradation in signal performance. As described in the Year Two Year-End Report, shunt capacitances measured at the inputs of the encapsulation signal leads degrade the transmission line characteristics of the signal string interconnects by creating a local decrease in impedance, which causes negative wavefront reflections to propagate to and fro along the signal string. Such reflections are always in the direction of the logic threshold, and hence decrease signal noise margins to some extent.

Though not described in detail in the Year Two Report, series inductances in the package leads also degrade overall system performance, but through a different mode of action. The shunt capacitance problem is becoming so well known that it is often stated that, given the choice between an improvement (i.e., a decrease) in shunt capacitance and an improvement (i.e., a decrease) in series inductance, design tradeoffs should favor the decrease in shunt capacitance. It is commonly assumed that, while shunt capacitance on the input of the encapsulation degrades waveform integrity thoughout the entire signal string, series inductance only contributes a constant time delay as the signal enters or leaves the encapsulation. It is usually stated that the inductance adds a delay approximately equal to the L/R time constant of the inductance in series with the resistance of the remainder of the signal string, but otherwise does not degrade the signal.

This assumption is valid for mainframe computer design, in which system clock rates are relatively low and overall signal propagation delay is of primary interest. However, in those instances in which system clock rate is extremely high, the number of gate stages between pipeline registers is relatively low (15 or less), and series inductance dominates any residual parasitic capacitances, a quite different phenomenon related to this series inductance problem occurs. This unusual behavior

becomes apparent when the interclock interval decreases to the point at which the duration of half a clock cycle is approximately equal to or less than 3 L/R time constants. The actual signal swing amplitude then begins to decrease, because the signal voltage applied to the outer end of the lead inductor will not have an opportunity to rise to its full value across the transmission line termination resistor before the gate drive voltage phase reverses, thereby driving the signal back in the other direction. Series parasitic inductances of 5-10 nH and transmission line termination resistances of 50-75 ohms result in L/R time constants in the range of .07 - .2 nsec; three such time constants are in the range of .2 - .6 nsec. Systems whose clock frequencies are greater than approximately 800 MHz will experience a decrease of signal swing and hence a loss of system noise margin, a phenomenon usually observed first in fanned-out clock signals. If lead series inductance rises to 15 nH, systems with clock rates above 550 MHz will suffer a loss of system noise margin. At 20 nH lead series inductance, systems with clock rates above 400 MHz will suffer a similar fate.

Noise margin losses can actually be worse than indicated above, because the signal risetimes and falltimes are not zero; the risetime/falltime delays must be convolved with the L/R time constant effects to ascertain the clock frequency at which signal degradation first occurs. For a .7 nsec signal risetime, problems are first noticed at clock rates of 250-450 MHz. As a

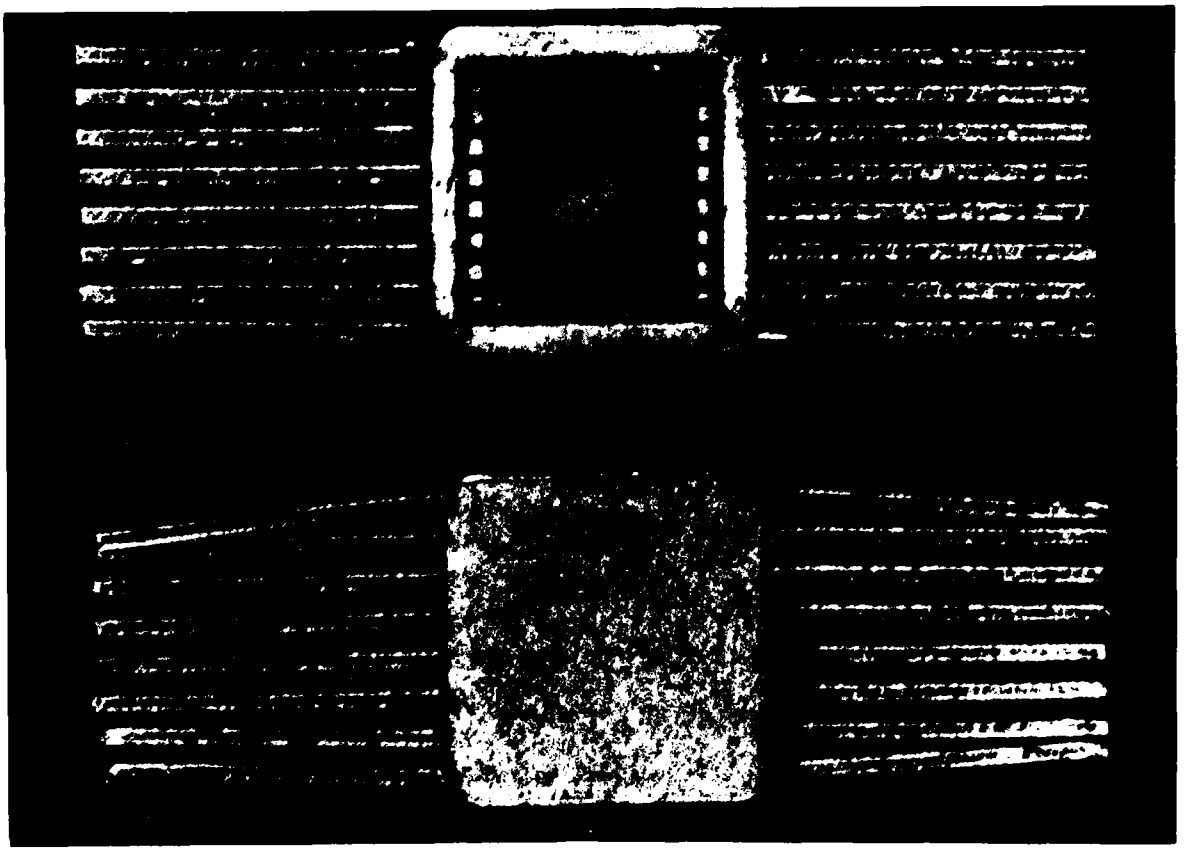
result, it is vital that both the inductive and capacitive parasitic reactances be minimized or balanced against each other (to form a transmission line) in the design of suitable encapsulation for high-speed systems.

Electrical Impedance Analysis Testing of Commercially Available Leadless Chip Carriers, Dual In-line Packages, and Connectors

The Hewlett Packard Model 4191A wide band impedance analyzer is capable of measuring parasitic capacitances in the femtofarad range and parasitic inductances in the picohenry range, over frequencies from 10-1000 MHz. We measured electrical characteristics of a variety of commercially available encapsulants; these devices will be discussed in order of increasing pin count.

Figure 2 depicts a front and rear view of a small 16-pin leaded flat pack currently in use for the encapsulation of small Gallium Arsenide integrated circuits. The small flat pack has been employed because of the ease of testing this structure, and because the package is reputed to have very low parasitic reactances. Because flat packs have traditionally been assumed to exhibit the highest performance of all such devices (except perhaps recently for leadless chip carriers), this part type and one of the commercial leadless chip carriers may serve as a reference for the performance of other devices with higher pinout counts. Figure 3 depicts measurements of the signal trace series

inductance, series resistance, and intertrace shunt capacitance on the Mini Systems Corporation Part #3H16M-1 16-lead flat pack. The measurements were performed in a cylindrical Faraday Cage, with the residual fixturing inductances and capacitances compensated automatically by the impedance measurement equipment. The average signal trace series inductance is approximately 2.25 nH for that portion of the signal line inside the package, plus an additional .2 inch length external to the package, i.e., that length of trace which must be bent down to the circuit board for



SMALL LEADED FLAT PACK USED TO ENCAPSULATE EXPERIMENTAL GaAs INTEGRATED CIRCUITS.

Figure 2

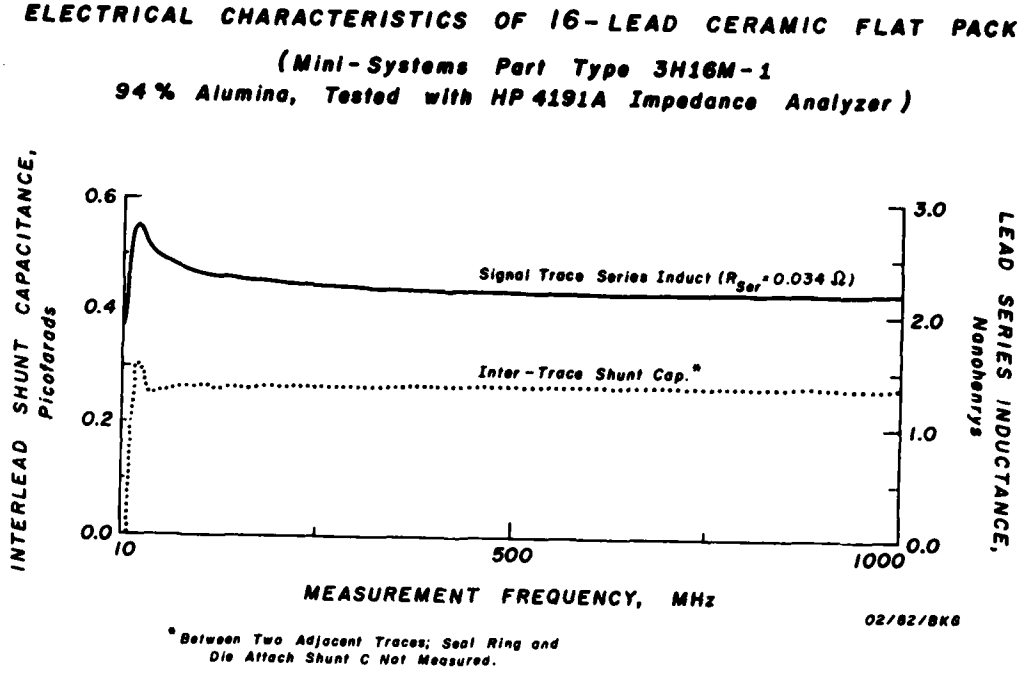
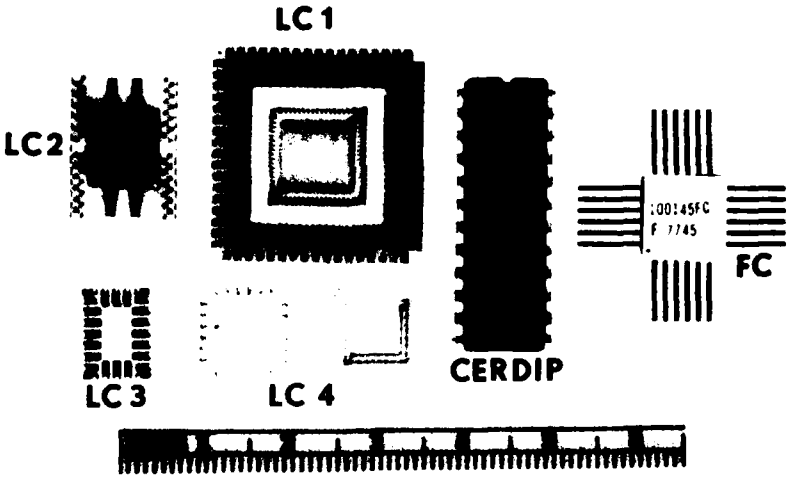


Figure 3

solder attachment. The intertrace shunt capacitance was measured between two adjacent traces; hence, an incoming signal wavefront would actually observe a trace parasitic shunt capacitance twice that indicated on this graph, i.e., about .5 pF. Both of these parasitic values are extremely low, as will become apparent later. The small peaks which appear at 10 MHz in both the inductance and capacitance curves are a resonance phenomonen between the inductive and capactive reactances at that frequency; since the 10 MHz range is well below any frequencies of interest for the systems under consideration, this low frequency resonance phenomenon is not considered to be a serious problem.

The second encapsulant, which appears to be one of the best commercially available such devices, is a small leadless chip carrier previously reported in our Year Two Year-End Report. This 400 x 400 mil chip carrier is labeled LC4 in the lower left corner of Figure 4; its capacitance and inductance characteristics are plotted in Figure 5. Note that signal trace series inductance is approximately 1.5 nH, somewhat lower than that for the 16 lead ceramic flat pack. The intertrace shunt capacitance of .3 pF is approximately the same as that for the 16 lead flat pack. Again, the actual value which would be observed by a



VARIOUS PACKAGES IN USE OR UNDER CONSIDERATION FOR SUBNANOSECOND ECL. FC = CERAMIC FLAT PACK CERDIP = 24-PIN CERAMIC DUAL IN-LINE PACKAGE: LC1-LC4: FOUR STYLES OF CERAMIC LEADLESS CHIP CARRIER.

FIGURE 4

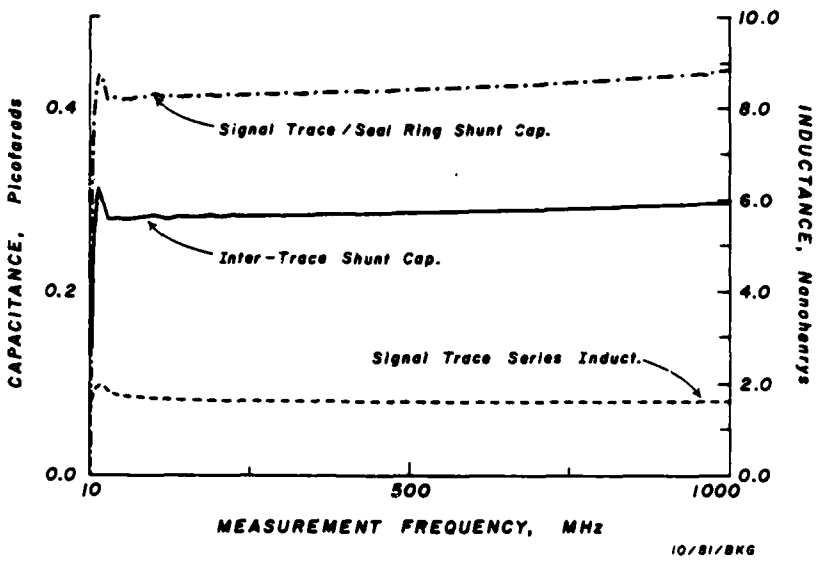


FIGURE 5

signal external to the package is twice this value, since the signal trace is exposed to shunt capacitance effects from both of its neighboring signal traces.

One additional measurement presented in Figure 5 is the signal trace to seal ring shunt capacitance, a value which by itself is larger than the intertrace shunt capacitance and hence adds significantly to the overall lead shunt capacitance. In fact, an additional capacitance path exists for each signal trace, i.e., between the signal trace and the seal ring, and then between the seal ring and the next adjacent traces; the intertrace shunt capacitance thus actually contains a component

ELECTRICAL CHARACTERISTICS OF
CERAMIC DUAL INLINE PACKAGE SIGNAL LEADS
(Die-Free Wide Body KC 402SD Glass 400 mil DIP
Tested with HP 4191A Impedance Analyzer)

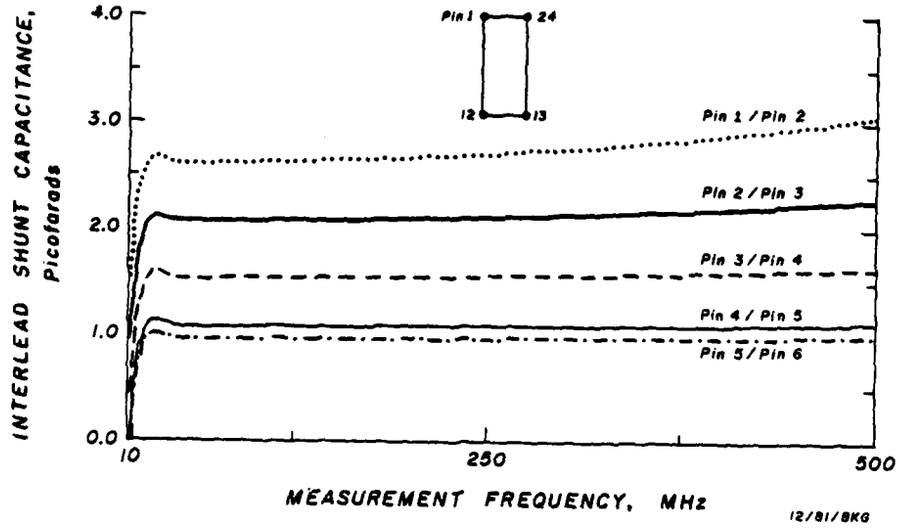


FIGURE 6

ELECTRICAL CHARACTERISTICS OF
CERAMIC DUAL INLINE PACKAGE SIGNAL LEADS
(Die-Free Wide Body KC 402SD Glass 400 mil DIP Tested
with HP 4191A Impedance Analyzer)

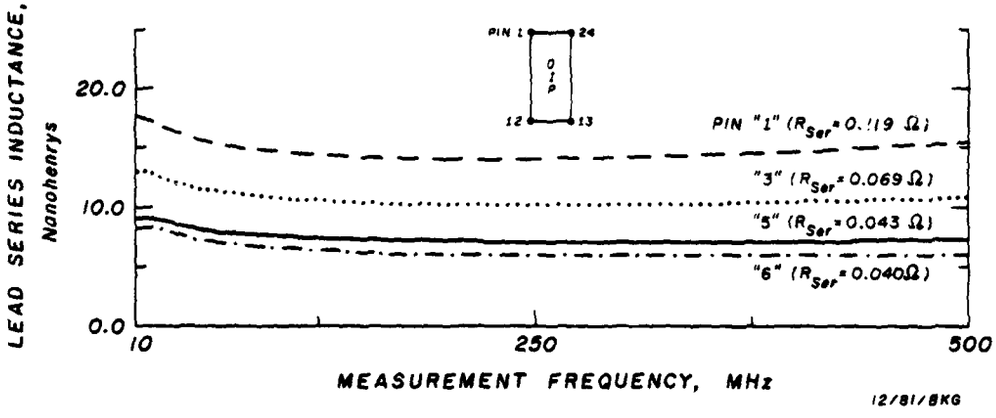


FIGURE 7

of signal trace-to-seal ring shunt capacitance. The reduction or elimination of the signal trace-to-seal ring shunt capacitance is feasible; removal of the seal ring would decrease the trace shunt capacitance to half its present value. Efforts to eliminate the seal ring on the Mayo-designed leadless chip carriers will be described later in this report.

The results of Figure 5 represent by far the best performance observed to date for any commercially available leadless chip carrier. Examination of the structure of this small leadless chip carrier (manufactured by 3M Corporation) leads to the conclusion that its good electrical performance occurred by happenstance rather than by intent; the device was designed for low power integrated circuits from which fast wavefronts were not expected. Because of the satisfactory electrical characteristics of this commercially available leadless chip carrier, it has been used at Mayo Foundation as an interim package until the Mayo-designed leadless chip carriers could be developed and refined. For example, in an interactive effort with Rockwell International Microelectronics Research and Development Center, this chip carrier has been employed for the packaging of Gallium Arsenide digital integrated circuits; the package has performed adequately for these early tests.

The next encapsulant to be examined was the 24-pin 400 x 1200 mil ceramic dual in-line package which has been used for SSI and MSI subnanosecond ECL integrated circuits. The package

tested at Mayo Foundation is, in fact, an improved version under investigation by Fairchild Camera and Instrument Corporation. The difference between the package which was tested at Mayo Foundation and the commercial version is the glass frit which seals the lid to the package; an improved material, KC-402, exhibits a lower dielectric constant, and hence minimizes interelectrode capacitance. This package also appears in Figure 4.

Figures 6 and 7 depict the measurements of interlead shunt capacitance and series inductance for various pin locations in this package. In each case shunt capacitance was measured between two adjacent pins; hence, except for pins 1, 12, 13, and 24, the actual capacitance observed by a data signal would be the sum of the capacitances to both pins adjacent to the one under test. Note the gradually decreasing values of shunt capacitance from pin 1/pin 2 to pin 5/pin 6, i.e., as measurements are made for pins closer to the center of the package. The run lengths for pins in the corners of a dual inline package are considerably greater than for those pins in the center of the package, resulting in widely varying values of parasitic reactances among the pins. Note that pin 2 observes a total shunt capacitance of approximately 5-6 pF, while pin 6 observes a total shunt capacitance of approximately 2 pF, i.e., a 3:1 difference.

These widely varying values of parasitics imply that signal strings connecting end pins of a dual inline package will exhibit poorer electrical performance, particularly regarding signal

risetimes, than will center pins; we have observed such behavior in actual operational tests. For a 500 MHz fundamental component of a rapid risetime signal, i.e., the value typical for high-speed ECL, an additional shunt capacitance of 2 pF across a 75 ohm transmission line decreases the local impedance of the line at that location to 51 ohms; similar measurements made for a 5 pF point load across the same transmission line results in an impedance decrease to 45.4 ohms. For a nominal 75 ohm transmission line, these shunt capacitances decrease the effective impedance of the transmission line by 32% and 39% respectively, resulting in voltage reflections at these locations of approximately 16% and 19.5% respectively; all such reflections will be in the direction of signal threshold, thereby directly decreasing system noise margins.

Figure 7 demonstrates the most serious disadvantage of these large dual inline packages; pin 1 series inductance values of 15 nH, and pin 6 series inductances of 8 nH, present series inductive impedances to a 500 MHz fundamental component of 47 ohms and 25 ohm respectively. Since these inductances are in series with a 75 ohm resistance, in effect they abstract 25-40% of the total signal swing from the fundamental component, and much higher percentages of the second, third, and fourth harmonics. These results indicate that the 24-pin dual inline packages are really unsuitable for high-speed ECL devices; CERDIPs have been employed primarily because of industry familarity with the advantages of

these structures, but without an equal awareness of their disadvantages. These results confirm our findings in the Year Two research that a substantial performance gain would be evident in a conversion from dual inline package encapsulation to leadless chip carrier encapsulation; comparison of Figure 5 with Figures 6 and 7 indicates that the electrical parasitics in the CERDIP structures are 5-10 times more severe than for the smallest LCCC devices. Dual inline packages larger than those tested here have not even been considered for high performance integrated circuits, whether silicon or Gallium Arsenide, and have not been tested.

Impedance analyses were conducted on a variety of larger leadless chip carriers. We measured the electrical characteristics of two versions of perhaps the best known of all the JEDEC packages, i.e., the JEDEC 68 contact Leadless Type A LCCC; these results appear in Figures 8 and 9. The 68-pad JEDEC LCCC is manufactured in two slightly different versions. In one version, the signal traces are wide, with only a minimal dielectric guard band between each trace. In the other form, the guard bands and the signal traces are of equal width.

Figure 8 depicts measurements made on a 68-pad LCCC with narrow traces; the corner and center traces exhibit 1.7 pF and 1.0 pF shunt capacitances respectively; in a 68-pad LCCC with wide traces, shunt capacitances for both corner and center pins

are closer to 2 pF. The higher shunt capacitance in the leadless chip carrier version with wide traces can be attributed to the increased coupling between traces with narrow guard bands.

To a first approximation, trace width is not a major determinant of lead series inductance; lead inductance is approximately one nH for each 100 mils of trace length. Figure 8 presents measurements of the series inductance of four signal traces, from the center of an edge of the 68-pad chip carrier to the corner; the series inductance of each trace increases steadily from 4.5 nH to 7.5 nH. The corner traces are longer than the center traces

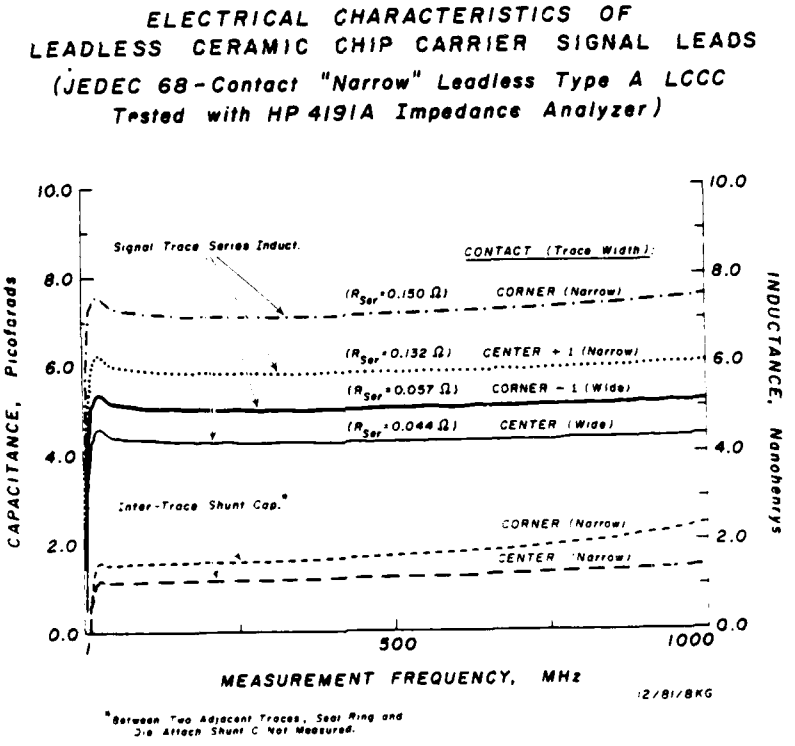


FIGURE 8

ELECTRICAL CHARACTERISTICS OF
LEADLESS CERAMIC CHIP CARRIER SIGNAL LEADS
(JEDEC 68-Contact "Wide" Leadless Type A LCCC
Tested with HP 4191A Impedance Analyzer)

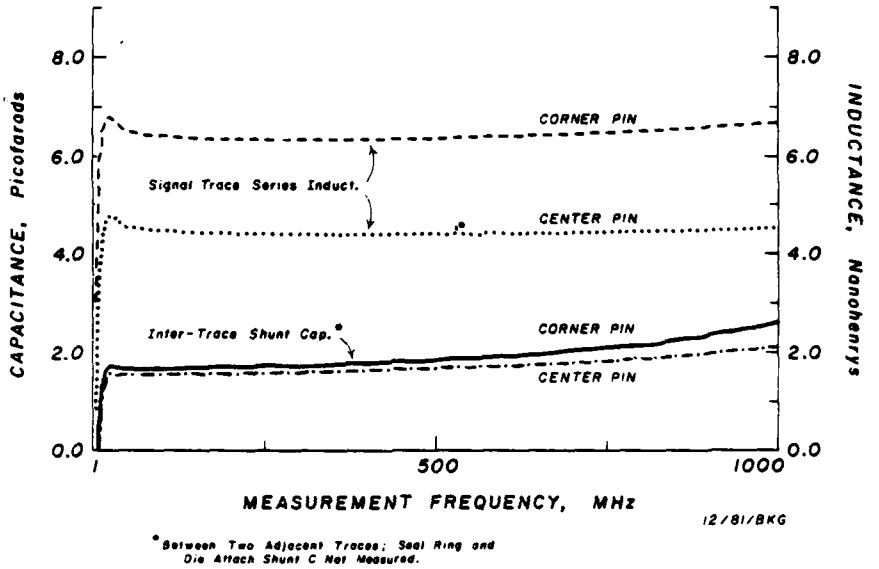


FIGURE 9

because of the diagonal path which they follow from the outer edge of the LCCC to the inner edge of the die well cavity. In no case does the series resistance of any of the traces exceed .2 ohms. These results typify the characterizations of commercially available large leadless chip carriers; their electrical characteristics and physical construction make them unsuitable as encapsulation for high performance integrated circuits (see the discussion in a following section entitled: A Final Look at Commercial Chip Carriers -- Do They Exhibit Controlled Line Impedances or Not?).

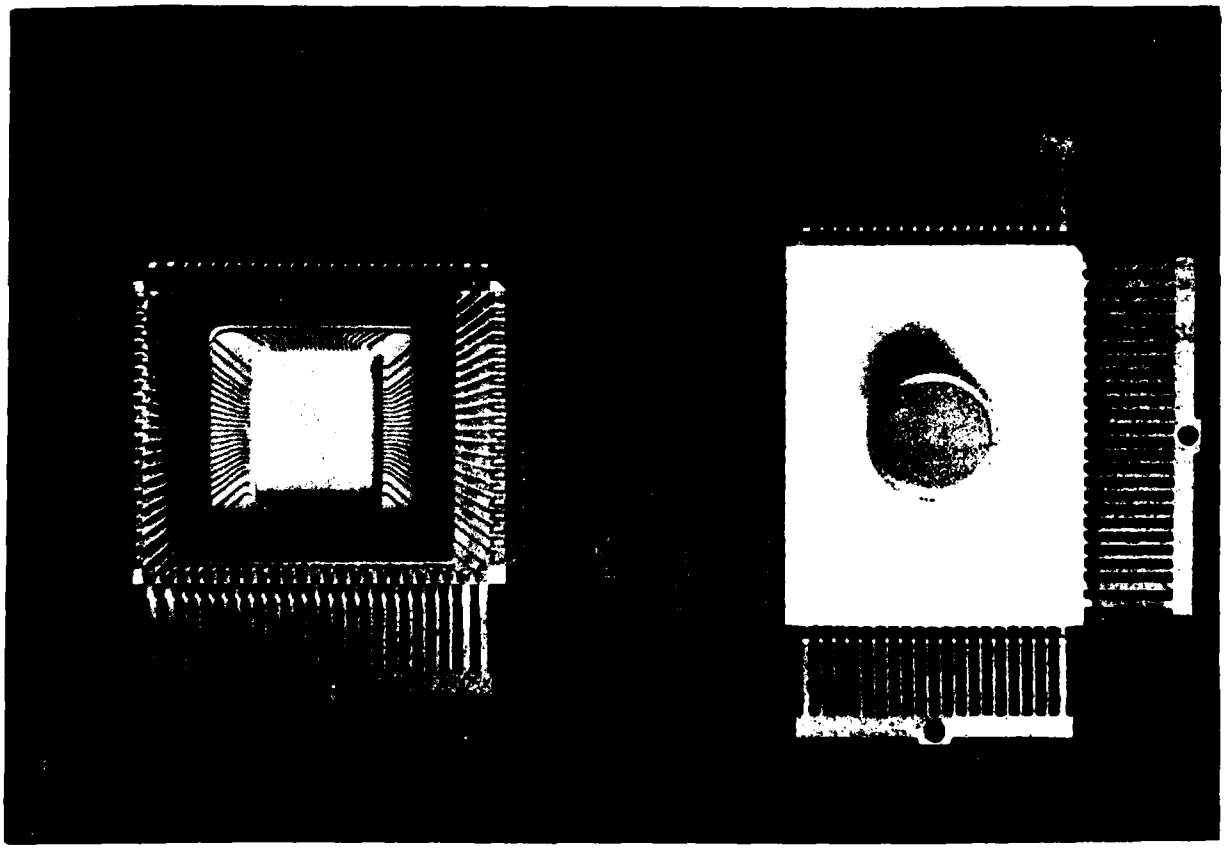
As a result of communications with the Radar Signal Processor Development Group at Hughes Aircraft, El Segundo, California, we were able to perform electrical characterization

tests on a 90 lead flat pack especially designed for high-speed LSI ECL components to be incorporated into a real time radar signal processor. Front and back views of the colleted, heat-sinked ceramic flat pack (with the lead frame intact) appear in Figure 10; for the electrical measurements presented in Figure 11, these leads were trimmed to approximately .1 inches in length, specified by Highes Aircraft to be the typical trimmed length prior to soldering of the leaded flat packs onto a multi-layer circuit board. The shunt capacitances for the corner and center traces, of approximately 1.25 pF and .75 pF respectively, are reasonably well controlled; even with a doubling of these values to the levels actually observed by a signal, i.e., 2.5 pF and 1.5 pF respectively, this package has an extremely well controlled shunt capacitance in spite of its large physical size. Conversely, the corner and center trace series inductances of 8 nH and 4 nH, respectively, indicate that the large size and long signal runs of this package do present an impediment to the traversal of fast risetime signals.

Figure 12 depicts a pair of large experimental leadless chip carriers containing 80 and 180 pads respectively, which were under consideration for use as encapsulants for large silicon ECL gate arrays. The 180-pin leadless chip carrier depicted on the right of Figure 12 was characterized in our laboratories; the results are depicted in Figure 13. Intertrace shunt capacitances for the corner and center traces are approximately 2.5 pF and 2 pF respectively; conversely, the corner trace and center trace

series inductances are 15 nH and 12 nH respectively, the highest series inductances measured in all packages tested. Series resistances are also quite high at .56 ohms and .49 ohms respectively, but are not of particular concern.

The shunt capacitance recordings reveal an interesting phenomenon which can be an additional concern at very high frequencies; note that the shunt capacitance rises rapidly above 750 MHz; inspection of the series inductance traces indicate that they also rise at frequencies above 750 MHz. These results indicate the occurrence of a parallel resonance between the parasitic



PROPRIETARY 90-LEAD FLAT PACK DESIGNED TO ACCEPT HIGH POWER ECL LSI COMPONENTS.

FIGURE 10

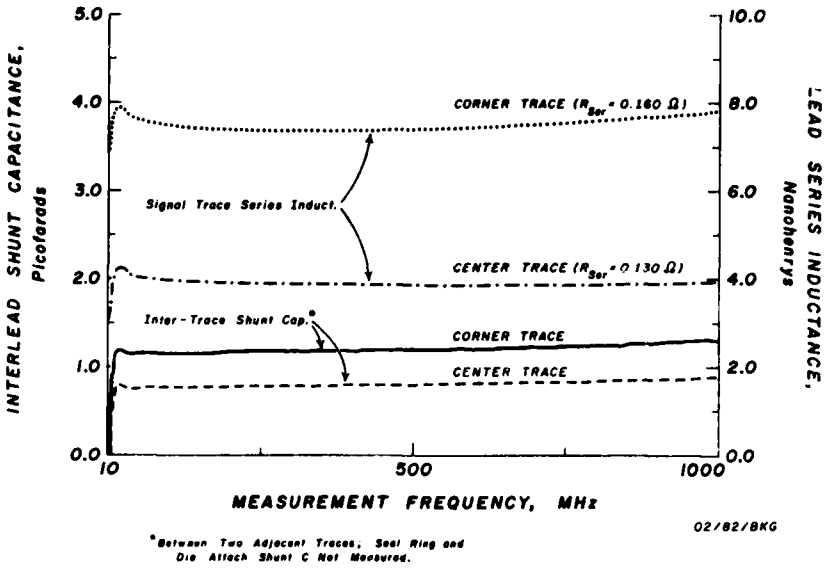
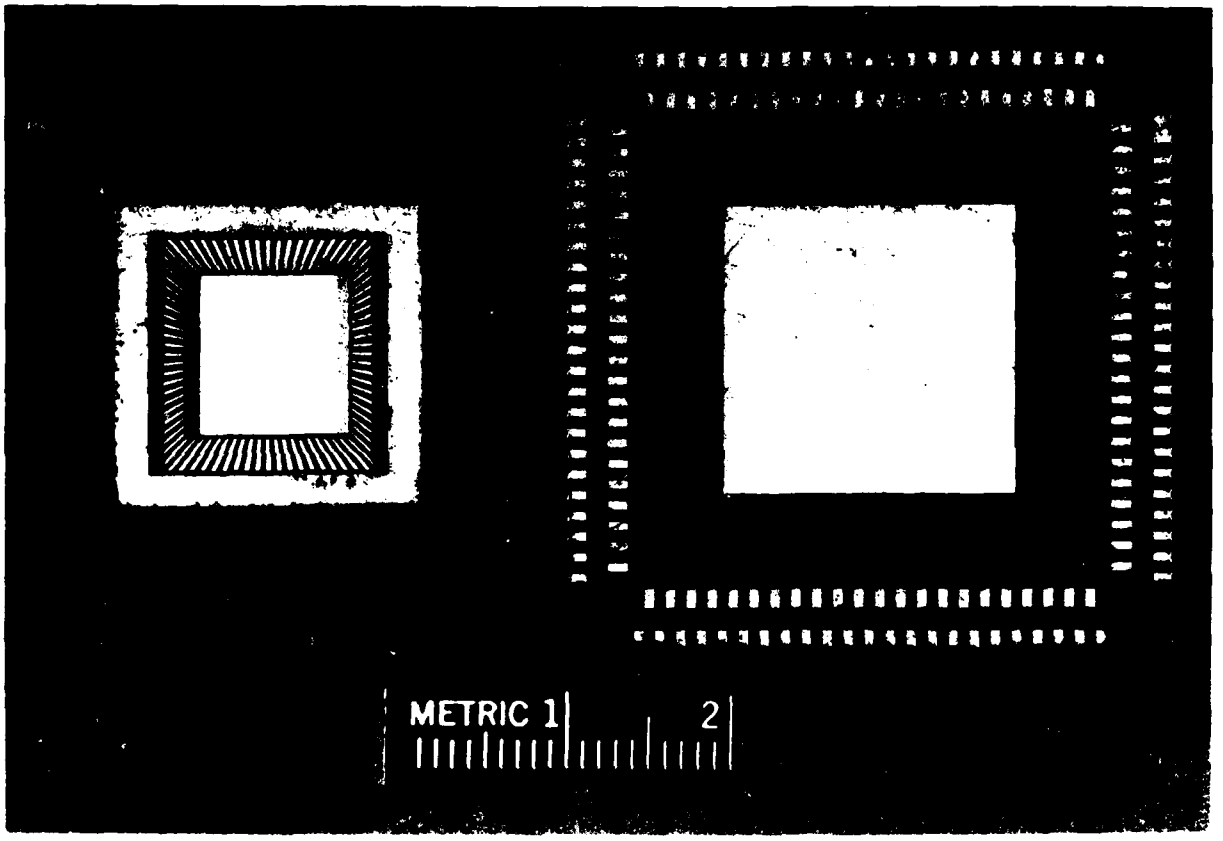


FIGURE 11

inductive and capacitive reactances; in this case, the resonance peak occurred at approximately 1.27 GHz. Although most such resonances occur in the 1-10 MHz range, parallel resonances at very high frequencies can cause the package to become completely blocking for those frequency components in the 1-2 GHz range. These phenomena must be accounted for during package design, or at least during the subsequent testing of packages to be used at these frequencies.

A package as large as the experimental 180 contact LCCC reported here is too large to achieve tight packing density on a logic board containing many high-speed devices and exhibits unacceptably high series inductances, thereby underscoring the

seriousness of the packaging problem, since packaging and encapsulation materials with very high pin counts must eventually be achieved. This 180-pin package did implement one mechanism for decreasing parasitic reactances in large packages, i.e., a minimization of overall package edge dimension through the use of two or more rows of contacts on 50 mil centers. Intercontact spacing could also be reduced, e.g., to 25 mils.



TWO EXPERIMENTAL LEADLESS CERAMIC CHIP CARRIERS. LEFT 80-PAD CARRIER. RIGHT: 180-PAD CARRIER WITH TWO ROWS OF CONTACTS.

FIGURE 12

ELECTRICAL CHARACTERISTICS OF
LEADLESS CERAMIC CHIP CARRIER SIGNAL LEADS
(Experimental 180-Contact Non-JEDEC LCCC Tested with
HP 4191A Impedance Analyzer)

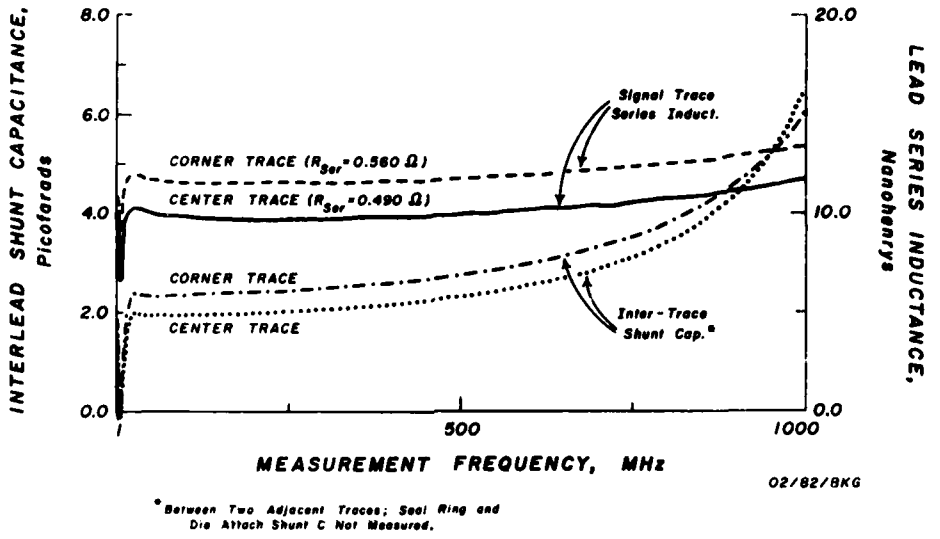


FIGURE 13

Connectors for Leadless Chip Carriers

The Year Two Year-End Report discussed the possible use of leadless chip carrier connectors to ease interchangeability of components on a circuit board, and reviewed several structures which had been investigated for this purpose. Although the HYPCON connector structure pioneered by Tektronix, Incorporated,

can be designed with very low levels of parasitic reactances, we have reported previously our inability to adopt this connector design to a very high packing density application, with two hundred or more integrated circuits on each logic panel. Conversely, we postulated that those connectors using metal-spring contacts and intended for tight packing on a logic board would have parasitic reactances too high to allow their use with high performance devices.

Figures 14 and 15 depict measurements of shunt capacitance and series inductance on several commercially available leadless chip carrier connectors for the 68-pad JEDEC Leadless Type A LCCC previously described. Photographs of these chip carrier connectors appear in the Year Two Report, on pages 112-114, Figures 40-43. Note that these parasitic reactances would be combined with, i.e., would add to, the parasitic reactances of the chip carriers themselves. The input shunt capacitances vary over a range of 3:1, with the low profile Augat connector exhibiting lead-to-lead shunt capacitances of .15 pF, (i.e., .3 pF actual shunt capacitance per active trace), while the AMP Corporation ADS surface mounted connector and the AMP Low Profile Connector exhibit shunt capacitances of .7 pF (1.4 pF) and .55 pF (1.1 pF) respectively. These shunt capacitances are not as large as had been expected.

CONTACT PIN SHUNT CAPACITANCE OF
SEVERAL CONNECTORS USED
WITH JEDEC 68-PAD LEADLESS TYPE A LCCC

(Measured Between Two Adjacent Contacts
with HP 4191A Impedance Analyzer;
Other Parasitics not Included)

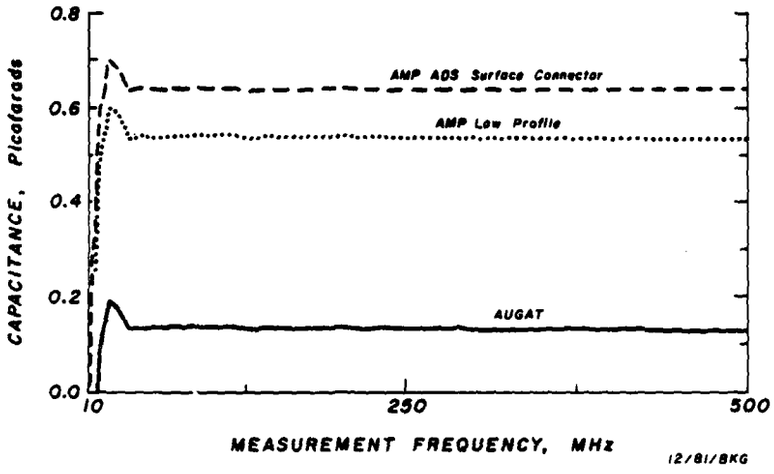


FIGURE 14

CONTACT PIN SERIES INDUCTANCE OF
SEVERAL CONNECTORS USED
WITH JEDEC 68-PAD LEADLESS TYPE A LCCC

(Measurements via HP 4191A Impedance Analyzer)

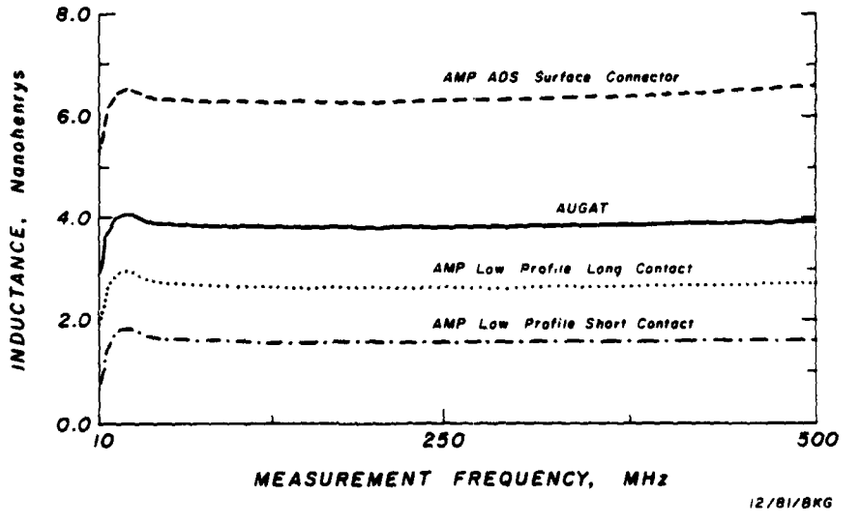


FIGURE 15

Series inductances measured in these connectors were approximately as expected; the AMP ADS Surface Mount Connector, with the largest contact pins and the longest signal paths, exhibits the highest series inductances at approximately 6.5 nH; the AMP Low Profile Connectors exhibit series inductances of 3 nH for the longer leads (on the corners of the packages) and slightly less than 2 nH for the center conductors. Since these series inductances would be directly additive with the 10-15 nH already measured in the leadless chip carriers themselves, an unacceptably high series inductance would result. Hence, although the use of leadless chip carriers without connectors requires the carriers to be solder bonded to a circuit board, we now believe that this is simply one of the prices which will have to be paid to extract maximum performance from high performance dice and leadless chip carrier encapsulation.

A Final Look at Commercial Chip Carriers -- Do They Exhibit Controlled Line Impedances or Not?

There is an alternate way of regarding the shunt capacitance and series inductance of the signal traces of commercial chip encapsulants which yields additional insight into the problems caused by these parasitic reactances. Let us assume for purposes of discussion that the measured series inductances and combined shunt capacitances from all sources are uniformly distributed along the length of each signal trace. Such an assumption is not

strictly correct, since contributions to shunt capacitance from seal ring and die attach areas are heavily weighted toward the inner end of each chip carrier signal trace. The assumption of uniform distribution of the parasitics allows each signal trace to be considered as a transmission line of some characteristic impedance, although this impedance may be too low or too high to be useful in a high frequency system.

The impedance of a transmission line can be computed from

$$Z_0 = \sqrt{L_0/C_0}$$

where L_0 represents the inductance per unit length and C_0 represents the shunt capacitance per unit length. Assuming uniform L_0 and C_0 per unit length in the chip carrier interconnects, we can derive an approximate "characteristic line impedance" for each chip carrier from the data of Figures 3 through 13. For example, for the small LCCC whose reactances are plotted in Figure 5, $L_0 \approx 1.75$ nH, while

$$C_0 \approx 2(\text{intertrace shunt C}) + (\text{Signal trace-to-Seal Ring Shunt C})$$
$$\approx 2(.3\text{ pF}) + .4\text{ pF} = 1\text{ pF}$$

Hence, the line impedance of the signal leads of this package appears from the formula to be approximately 42 ohms. In fact, if this same calculation is performed on the CERDIP packages of Figure 6, the 68-pad JEDEC leadless chip carriers of Figure 8, or the 90-lead flat pack of Figure 11, the resulting

"impedances" all lie in the range of 48-54 ohms, quite close to the nominal value of 50 ohms used in most transmission line interconnects. However, these values do not indicate that the packages exhibit controlled, low impedances, for the following reason. For the shunt capacitances and series inductances reported in these figures to result in true transmission lines, the two traces on either side of each "driven" or "signal" trace would have to be maintained at A.C. ground potential; the impedance of a signal trace in any such transmission line structure is defined only with respect to an A.C. ground line or plane. For example, if the traces on either side of the "driven" trace were grounded, a coplanar transmission line would result, and the impedances calculated above would be valid. Conversely, if two adjacent traces were driven differentially, the impedance would be defined, though by a different formula and with different numerical values.

However, if all adjacent traces are driven single ended, and all randomly with respect to one another, the dynamic impedances of the traces are undefined, and actually assume various values depending on the instantaneous combination of rising and falling wavefront edges on adjacent traces. For example, if the signals on three adjacent traces are all undergoing a positive edge transition simultaneously, the effective shunt capacitance of the center trace will appear momentarily to drop to zero, since both ends of the capacitors in the L-C Pi-section ladder network representation of the transmission line would observe identical

instantaneous voltage values; the capacitors would thus not charge at all, and would behave like a succession of open circuits. From the previous formula, Z_0 would momentarily appear to be infinite; that is, in actuality the trace series inductance would completely dominate the capacitive parasitic effects. Conversely, if the logic level on the center trace were transitioning high and the levels on the two neighboring traces were transitioning low, the effective capacitance of the center trace would momentarily appear to be twice the actual value; the center trace line impedance would momentarily drop to half its calculated value.

The previous comments are not intended to be quantitative, but instead to indicate the possible range of prevailing conditions. Not only are the line impedances undefined, they vary unpredictably over wide ranges. Unless each of these leads is referenced to a true A.C. ground plane, it is misleading at best to consider them to be transmission lines. Only by providing an opposing ground plane, which was not done in any of the commercial chip carriers tested at Mayo, or by grounding every other trace to create a coplanar transmission line (which is also not usually done) can a constant impedance structure be guaranteed. These factors tend to reinforce our conclusions that commercial chip carriers are unsuitable for encapsulation of fast wavefront devices.

Based upon the factors described above, chip carriers for these applications should be designed with true transmission line leads. However, the most useful impedance value may not be a nominal 50 ohms or 75 ohms, in contradistinction to the comments appearing with increasing regularity in the literature; other values may result in an overall improvement of system function. A study of optimum impedances for chip carriers will be conducted in the next year of the project.

Thermal Tests of Commercially Available Chip Encapsulants

We wished to generate baseline thermal performance data of various chip encapsulants which could be compared to the Mayo-designed leadless chip carriers. Measurements were made of the outside case temperatures for different package styles in which had been installed several different types of ECL components. A small wind tunnel was fabricated into which could be installed a specially designed circuit board with its surfaces parallel to the air flow. The board was designed to accept at its center the installation of a ceramic flat pack, leadless chip carrier, or dual inline package, with or without a heat sink. The edges of the circuit board extend beyond the cylindrical walls of the wind tunnel, thereby allowing its signal traces to be employed for the connection of thermocouple leads and voltage and ground lines to power the integrated circuit. Current flow to the chip, power

THERMAL BEHAVIOR OF ENCAPSULATION FOR HIGH POWER INTEGRATED CIRCUITS UNDER VARIOUS OPERATING CONDITIONS

(100102 ECL Component; 24-Pin Ceramic Flat Pack; ~ 1500 LFPM Air Flow*; Dual Thermocouple Sensing)

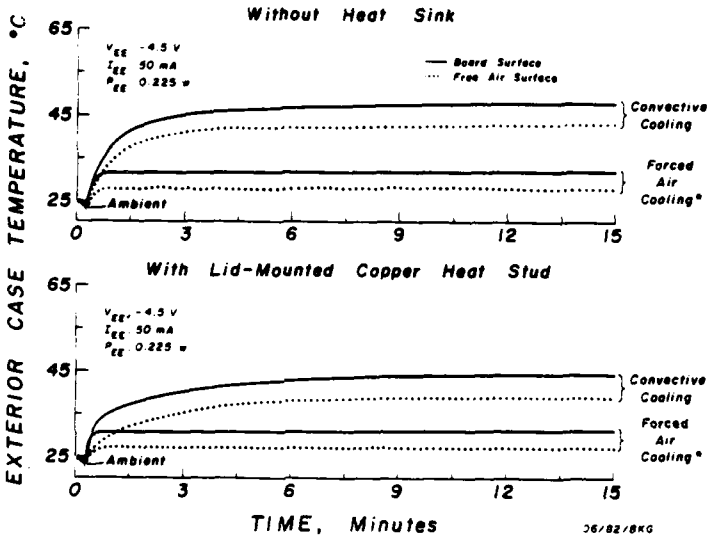


FIGURE 16

supply voltage, and dissipated power were measured continually (however, since these parameters did not change, they are reported as fixed values).

Each component was solder bonded to the test circuit board; all true and complement outputs were terminated in 85 ohms, and hence created a condition of maximum on-chip power dissipation. Thermocouples were mounted on both sides of the encapsulation,

i.e., one between the package and the circuit board and the other on the free air side of the encapsulant. For several studies a small cylindrical copper heat stud 187 mils in diameter and 750 mils in length was solder bonded or epoxy bonded to the appropriate surface of the encapsulant (not always the free air surface). ECL integrated circuits were used for these tests because, unlike TTL integrated circuits, the power dissipation of ECL devices is independent of clocking frequency. All thermal measurements could thus be made with only the supply voltages applied; the long signal runs on the supporting circuit boards did not introduce any systematic errors.

Measurements were made on commercially available 24-pin ceramic leaded flat packs of the type designated by Fairchild Camera and Instrument Corporation as their 4Q package, on the 3M Corporation 88ST524AC 24-pad 400 mil square leadless chip carrier, and on the 24-pin ceramic dual inline package which Fairchild Camera and Instrument Corporation designates as their 6Q package. Whenever possible, these measurements were performed on several examples of the same package so that an effective thermal resistance to the cooling medium could be derived in °C/watt, with or without the heat sink. Figure 16 typifies the results of these measurements. The upper and lower exterior surfaces of the encapsulants were recorded for periods of 15 minutes, with initial measurements recorded at ambient temperature. Both still-air convective cooling and forced air cooling were

used; measurements were made with and without a lid-mounted or base-mounted copper heat stud. Lid mounting of the copper heat stud provides an inefficient thermal path. Unfortunately, many of the commercially available leadless chip carriers can only be mounted lid-up to the air stream; as a result, it was necessary to acquire thermal data in this configuration as well. The 24-pin leaded flat packs can be mounted either lid-up or base-up; since they are approximately the same size as the smaller leadless chip carriers, they serve as a useful model for lid-up versus lid-down mounting for ceramic structures of 500 mil edge dimension or less.

THERMAL BEHAVIOR OF ENCAPSULATION FOR HIGH POWER INTEGRATED CIRCUITS UNDER VARIOUS OPERATING CONDITIONS

(100151 ECL Component ; 24-Pin Ceramic Flat Pack ; — 1500 LFPM Air Flow; Dual Thermocouple Sensing)*

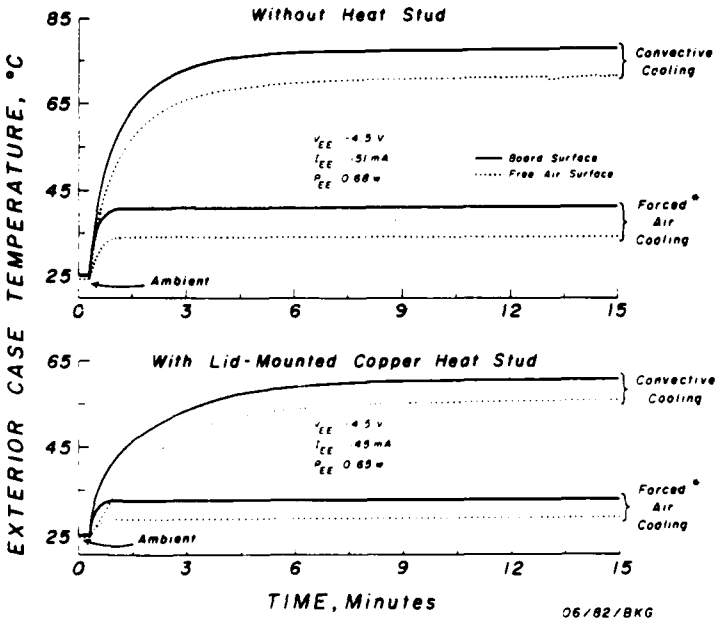


FIGURE 17

Figure 16 depicts results from a 100102 SSI component, with a power dissipation of 225 mW; even with convective cooling and no heat sink, and with the flat pack mounted lid up to

THERMAL BEHAVIOR OF ENCAPSULATION FOR HIGH POWER INTEGRATED CIRCUITS UNDER VARIOUS OPERATING CONDITIONS

(100151 ECL Component; 24-Pin Ceramic Flat Pack; ~1500 LFPM Air Flow*; Dual Thermocouple Sensing)

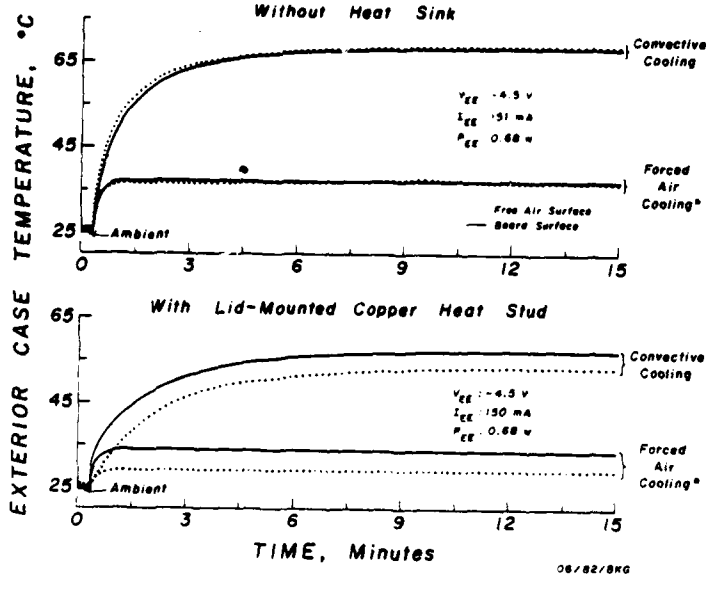


FIGURE 18

the air stream, package temperature reaches approximately 47°C; with convective cooling, the final temperature is approximately 35°C. These charts must be reviewed carefully, because the critical temperature is always that closest to the die, which itself may either be closest to the logic board or facing the air stream in different studies. In Figure 16, the ECL die was closest to the board surface; hence the board surface thermal measurements, not the free air measurements, are the important ones. Figure 17 depicts measurements of a 100151 ECL component, dissipating approximately .68 watts; here the ECL dice, which is closest to the logic board surface, reaches approximately 67°C without a heat stud and 60°C with a lid mounted copper heat stud. A second 100151 was tested (Figure 18), with similar results.

Similar measurements were then made on a 100136 4-bit counter dissipating approximately one watt. In Figure 19 we see that the case temperature, closest to the ECL dice and the board in this experiment, exceeds 95°C with convective cooling; 45°C with forced air cooling without a heat sink; 70°C with convective cooling and a heat sink; and 37°C with forced air cooling and with a lid mounted copper heat stud. Figure 20 shows simi-lar results from a second 100136 in a ceramic flat pack.

Figure 21 depicts similar results for a 100151 ECL component packaged in a 24-pin leadless ceramic chip carrier; this chip carrier can only be mounted with the lid facing the air stream, and the ceramic surface (the surface supporting the die itself)

closest to the logic board. Figures 22 and 23 depict equivalent thermal measurements for a 24-pin dual inline ceramic encapsulation, with a 100151 component dissipating .63 watts, and a 100136 component dissipating 1.04 watts respectively. In this set of figures, the upper panels depict data measured without a heat stud; conversely, the lower panels depict measurements made with a copper heat stud mounted on the base of the dual inline

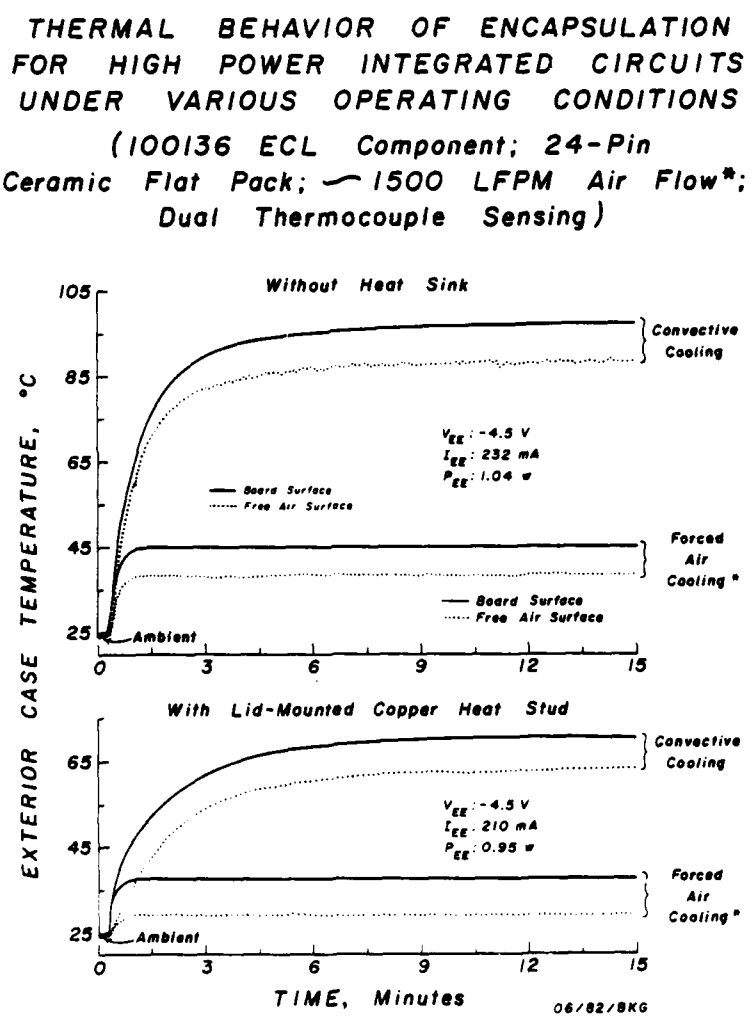


FIGURE 19

THERMAL BEHAVIOR OF ENCAPSULATION FOR HIGH POWER INTEGRATED CIRCUITS UNDER VARIOUS OPERATING CONDITIONS

(100136 ECL Component; 24-Pin Ceramic Flat Pack; — 1500 LFPM Air Flow*; Dual Thermocouple Sensing)

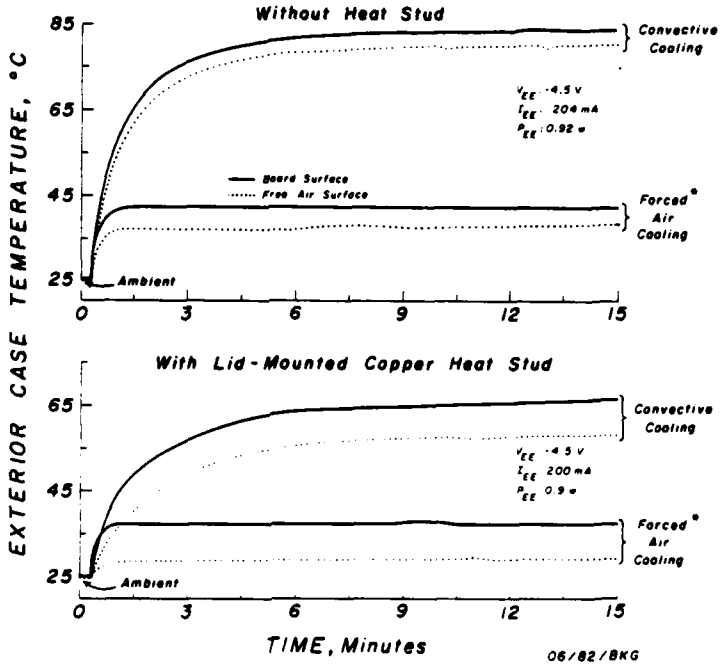


FIGURE 20

package (with the heat stud protruding through a small hole in the circuit board). Note the significant difference in final stabilized temperature with and without forced air cooling, and, in those cases where dual measurements were made, between the upper and lower surfaces of the chip carriers.

Figures 24, 25, 26, 27 depict similar types of thermal measurements recorded from ECL components packaged in 24-pin ceramic flat packs and a 3M leadless chip carrier; however, these

THERMAL BEHAVIOR OF ENCAPSULATION FOR HIGH POWER INTEGRATED CIRCUITS UNDER VARIOUS OPERATING CONDITIONS

(100151 ECL Component; 24-Pin 3M Leadless Chip Carrier; ~1500 LFPM Air Flow; Dual Thermocouple Sensing)*

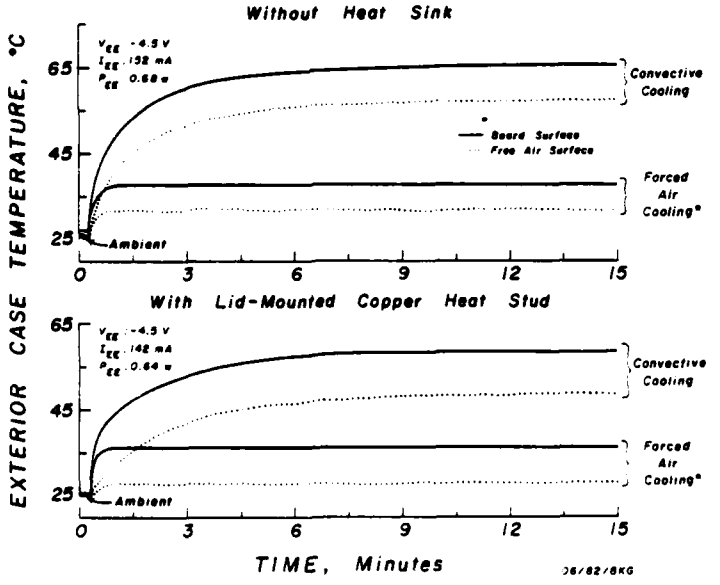


FIGURE 21

measurements were made with the ceramic flat packs mounted with the ECL die facing toward the air stream for optimum cooling. Thermal measurements were made in this mounting configuration with and without a heat stud. It was not feasible to invert the leadless chip carrier into a "ceramic side up" configuration because of its mechanical characteristics; to test the effectiveness of heat stud mounting on the die-facing ceramic surface, a small hole was drilled through the circuit board large enough to accomodate the copper shank. Figures 24 and 25 depict the measurements recorded from a 100101 SSI component and from a

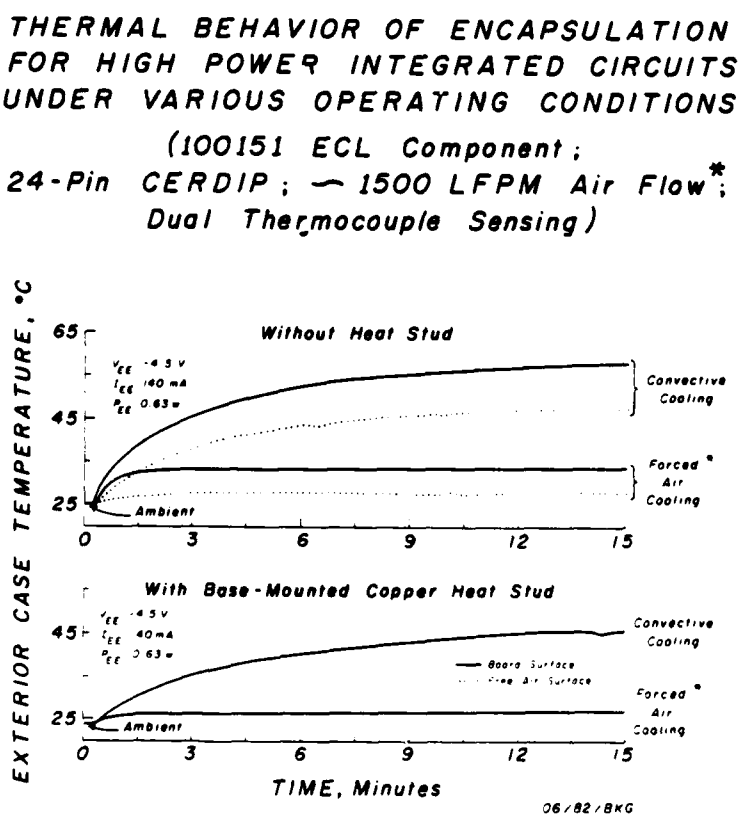


FIGURE 22

100151 register component, dissipating .225 and .58 watts, respectively; the temperatures achieved by the package surfaces (note that the free air surface is the surface closest to the die in these measurements) are higher without the heat stud than they

THERMAL BEHAVIOR OF ENCAPSULATION FOR HIGH POWER INTEGRATED CIRCUITS UNDER VARIOUS OPERATING CONDITIONS

(100136 ECL Component ; 24-Pin CERDIP; ~ 1500 LFPM Air Flow*; Dual Thermocouple Sensing)

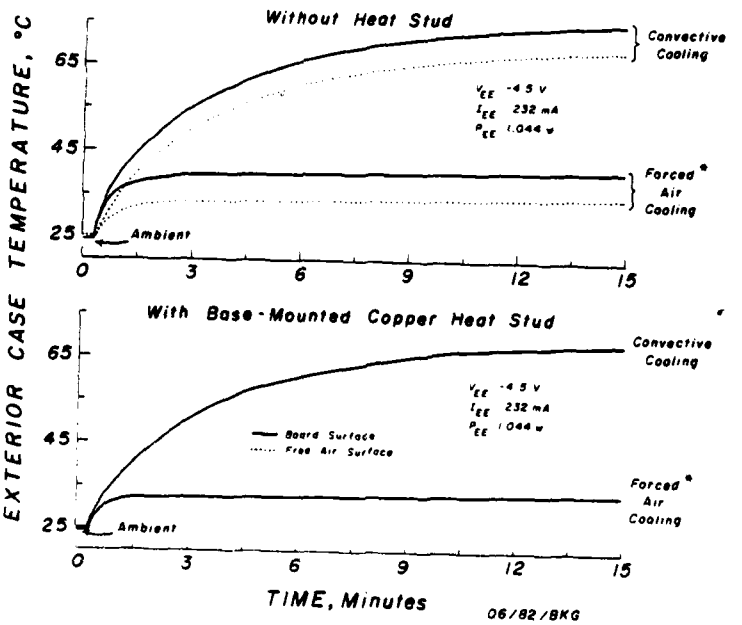


FIGURE 23

THERMAL BEHAVIOR OF ENCAPSULATION FOR HIGH POWER INTEGRATED CIRCUITS UNDER VARIOUS OPERATING CONDITIONS

(100102 ECL Component; 24-Pin; Ceramic Flat Pack; —1500 LFPM Air Flow*; Dual Thermocouple Sensing)

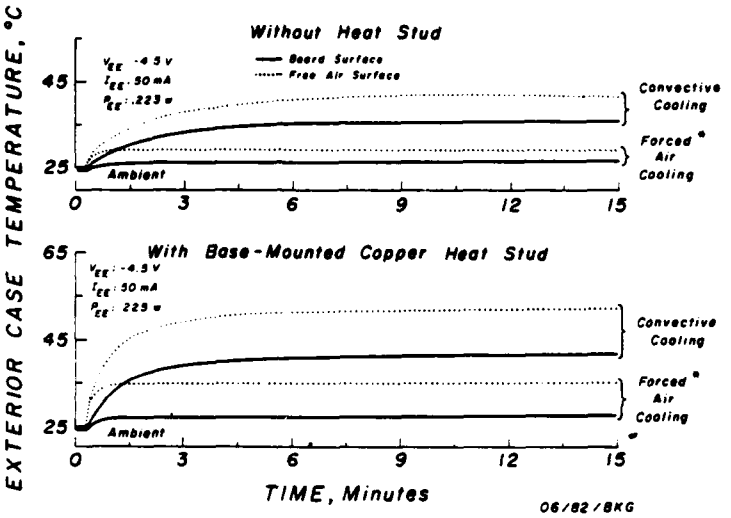


FIGURE 24

are with the installation of the heat stud, and that, as expected, both package surface temperatures are lower with forced air cooling than without cooling. Figure 26 shows equivalent results for a 100136 high-speed 4-bit counter dissapating .766 watts; in comparison to Figure 25, the same trends are observed, although with a temperature offset resulting from the higher heat dissipation.

Comparisons of these results are difficult to achieve, as a result of differences in the temperature measurement configurations on a variety of packages using a different thermocouples; the thickness of the conductive epoxy can create

THERMAL BEHAVIOR OF ENCAPSULATION FOR HIGH POWER INTEGRATED CIRCUITS UNDER VARIOUS OPERATING CONDITIONS

(100151 Component; 24-Pin Ceramic Flat Pack; ~1500 LFPM Air Flow* Dual Thermocouple Sensing)

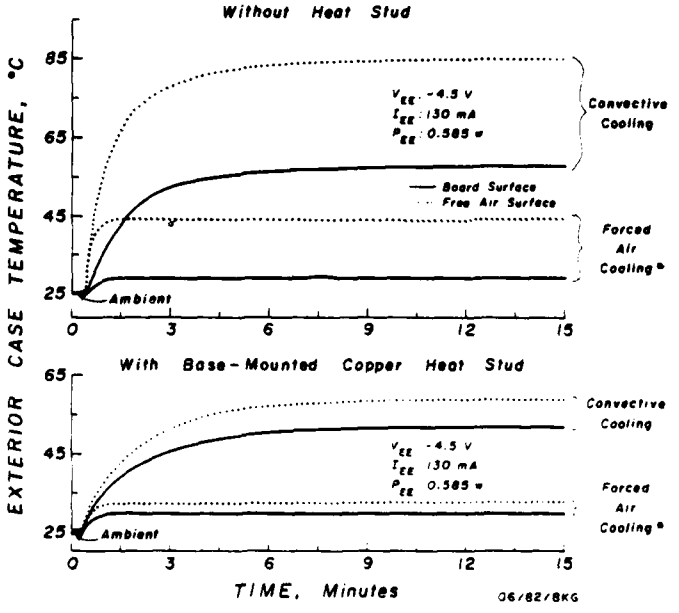


FIGURE 25

THERMAL BEHAVIOR OF ENCAPSULATION FOR HIGH POWER INTEGRATED CIRCUITS UNDER VARIOUS OPERATING CONDITIONS

(100136 ECL Component; 24-Pin; Ceramic Flat Pack; — 1500 LFPM Air Flow*; Dual Thermocouple Sensing)

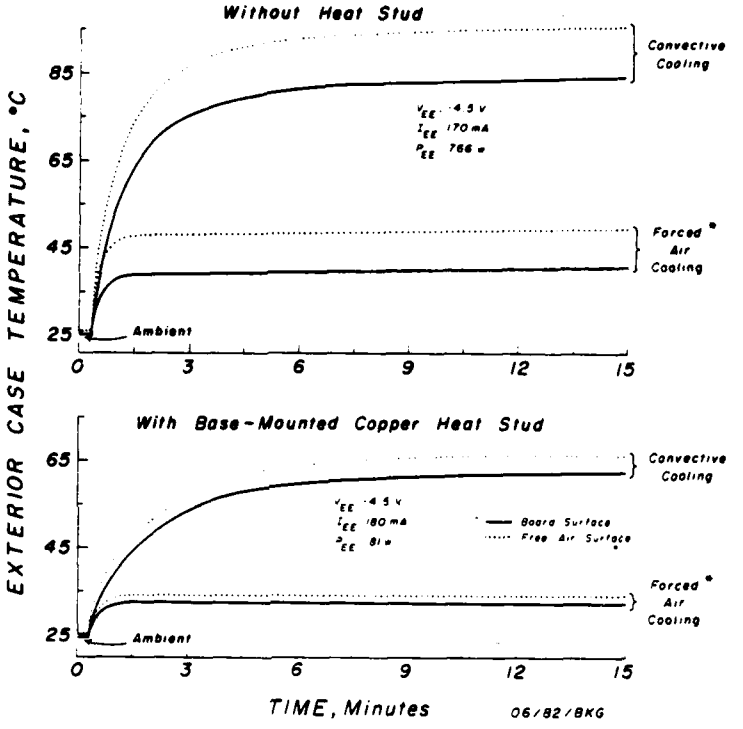


FIGURE 26

variations in thermal conductivity large enough to negate the advantages both of a heat stud and of the mounting configuration with respect to the air stream. In addition, leaded flat packs cool almost equally well either die-up or die-down because the leads themselves are a major source of thermal dissipation for these encapsulants. In general, we observed improved cooling and

THERMAL BEHAVIOR OF ENCAPSULATION
FOR HIGH POWER INTEGRATED CIRCUITS UNDER
VARIOUS OPERATING CONDITIONS
(100151 ECL Component; 24-Pad 3M Leadless Chip Carrier;
~ 1500 LFPM Air Flow*; Dual Thermocouple Sensing)

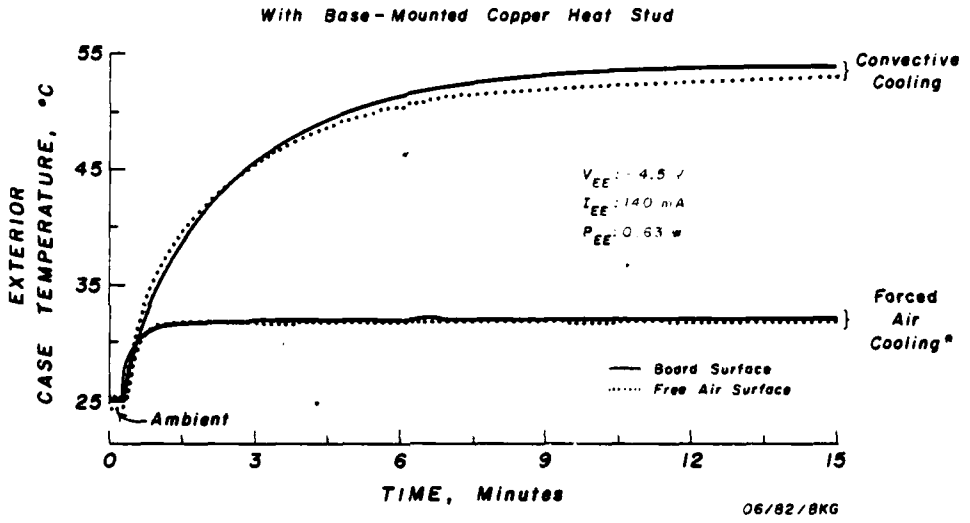


FIGURE 27

lower chip operating temperatures when a base mounted or even a lid mounted copper heat stud was used. Great care must be taken in the mounting of heat studs to any encapsulant to prevent the mounting technique from actually increasing the thermal path resistance.

Summary of Electrical and Thermal Measurements on Commercially Available Chip Encapsulants

In summary of the electrical and thermal measurements on commercially available chip encapsulants, the following elements are now clear. First, except for leadless chip carriers and leaded flat packs of very small edge dimensions, commercially available dual inline packages, large flat packs, and large leadless chip carriers are unsuitable for use with high frequency integrated circuits, because the high shunt capacitances and/or series inductances of the package lead degrade signal propagation and waveform conformation.

The results of the thermal measurements on leadless chip carriers underscored the difficulty of making reliable, repeatable measurements of the thermal performance of these packages because of the large number of uncontrolled variables from study to study. Better instrumentation is required which allows more repeatable measurements from package to package; it is also clear that ultimately an accurate in-package temperature sensor must be available for direct insertion into test parts intended for thermal study. The development of such a "thermal test chip" is currently being discussed with Fairchild Camera and Instrument Corporation.

The electrical measurements reported above have confirmed our comments in the Year Two Report that it would be necessary to develop a family of high performance leadless chip carriers. This is not an easy task; our initial development of a pair of small leadless chip carriers, described in the next section of this report, is merely the beginning of the effort.

Continuing Design Efforts for the Mayo Leadless Ceramic Chip Carrier

In the Year Two Report we described the development of a 32-pad leadless ceramic chip carrier optimized for use with high-power, high frequency silicon devices; these LCCCs were designed for air cooling by using a recessed lid with tungsten bumps serving as standoffs to allow removal of activating solder fluxes between the soldered LCCCs and the circuit board following vapor phase reflow solder bonding. The 32 contact pad specification was originally based upon the maximum cavity size which would be necessary to accommodate high-speed ECL components of SSI, MSI, and memory sizes, either already available or in planning stages. The outer dimensions of this leadless chip carrier were 450 mils by 550 mils, and, though larger than we would have liked, appeared sufficiently flexible to satisfy near and intermediate term needs for a small, high performance leadless ceramic chip carrier. In the Year Two Report, we pointed out several steps

which were taken in the design of the 32-pad carrier to minimize parasitic shunt capacitances and series inductances, including the use of wide guard bands on the bonding finger layer to minimize intertrace shunt capacitances, the elimination of plating fingers between the signal interconnections, the use of a single plating finger for the die attach area, and the incorporation of several penetrating vias to allow external capacitive decoupling of the internal power and ground layers.

As described earlier in this report, in July, 1981, after we had released the final designs to the offshore fabricator of these leadless chip carriers, Fairchild Camera and Instrument Corporation discovered an error in their calculation of maximal ECL component die sizes (particularly in regard to large static RAM components already in development). Based upon their corrected data, Fairchild engineers concluded that conversion to a smaller 28-pad leadless ceramic chip carrier might be feasible. The reduced area and increased board packing density of a smaller chip carrier appeared attractive to the Fairchild engineers, who requested us to consider a smaller chip carrier. After a review of the advantages and disadvantages of a redesign at such a late stage, the redesign effort was initiated.

For commercial reasons, the Fairchild group was strongly compelled to adopt a recently announced JEDEC standard footprint for small leadless ceramic chip carriers of 28 to 32 pins.

Comparison of the JEDEC footprint with the preferred Mayo design underscored substantial differences between the two approaches; only one of the designs could possibly survive the review process. A chip carrier with the JEDEC footprint was a long aspect ratio package of edge dimensions 350 mils by 550 mils, with nine contacts along the long edge and five contacts along the short edge. Conversely, the Mayo design, though also rectangular, exhibited a much shorter aspect ratio, with dimensions 400 mils by 500 mils, with six contacts on the smaller dimension of the carrier and eight contacts on its longer dimension. The JEDEC standards committee has advised against the use of an even number of contacts along any side, since there is then no "center contact" which can be used for assembly reference.

We compared the probable performance of the two designs, and presented these results to the Fairchild engineers. The results of this study demonstrated yet again that high frequency packaging design is generally not well understood in the industry, and the JEDEC standard package outlines appear not to be devised with the peculiar electronic constraints of high-speed integrated circuits in mind. Because this analysis illustrates the steps which must be taken from the outset of the design of a package intended for high performance integrated circuits, our study of these packages and the resulting performance tables will be presented in their entirety.

Mechanical Comparisons Between 350 x 550 MIL LCCC and 400 x 500 MIL LCCC

The long aspect ratio package preferred by Fairchild was a JEDEC standard footprint, while the short aspect ratio package recommended by Mayo was not. Footprint areas of the two proposed LCCCs were very similar: the footprint of the 350 x 550 mil LCCC was 192,500 mil^2, whereas the footprint of the 400 x 500 mil package was 200,000 mil^2; the footprint area is thus 4% larger for the short aspect ratio package. The long aspect ratio package wastes package real estate area at its two long ends; since the proposed die cavity was initially 165 x 200 mils, a small rectangle of 100 x 165 mils would have been wasted at <u>each</u> end, for a total area loss of 200 x 165 mils.

A long aspect ratio package would be subject to greater thermal-cycle induced mechanical stresses than necessary (by at least 10%) in the long direction than would the short aspect ratio package.[1]

Electrical Comparisons Between 350 x 550 mil LCCC and 400 x 500 mil LCCC

If the long aspect ratio package proposed by Fairchild had been selected, there would have been five contacts along each short edge, and 9 contacts along the long edge. Conversely, for

[1] J. E. Fennimore, Electronic Packaging and Production, December 1978, pages 128-132).

the short aspect ratio package proposed by Mayo, there would be six and eight contacts along the short and long edges respectively. For logic components, optimum electrical performance is achieved when differential input contacts are on adjacent pins, and differential output contacts are on adjacent pins. This is presently the bondout approach used for ECL logic dice designed for leaded flat packs of six pads per side, but would have been difficult with five pads on two edges. This issue was particularly relevant for the F100114 Differential Line Receiver and the F100125 ECL/TTL translator. In addition, memory components generally concentrate most of their bondout pads along or just adjacent to their narrow ends. The larger the aspect ratio of the package, the worse becomes the mismatch between the number of padouts on the memory components and the number of padouts on the chip carrier.

The measured electrical characteristics of commercially available LCCCs, at least to frequencies up to 1 GHz, can to a first approximation be normalized to electrical parasitic levels per 50 mils of bond length. Values presented in the accompanying tables assume for simplicity that both inductive and capacitive parasitics can be represented as LUMPED elements, although in actuality they should be represented as distributed parasitics.

a. Shunt capacitance between signal lead and die attach area: .0625 pF/50 mils length.

b. Shunt capacitance between signal lead and seal ring: .0875 pF/50 mils length.

c. Combined shunt capacitance, assuming lumped values, from all sources between signal lead and AC ground: .15 pF/50 mils length.

d. Series inductance of each lead: .5 nH/50 mils length.

At a fundamental frequency of 500 MHz (the situation will be more extreme for upper harmonics), these values can be roughly converted to impedance as:

a. Shunt capacitive reactance from all sources, assuming lumped capacitances, between signal and AC ground: 2.122×10^3 ohms/50 mils length.

b. Series inductive reactance of each signal lead: 1.57 ohms/50 mils length.

With the above numbers, assuming a 50 x 50 mil ECL die, the parasitics for center and corner pins for packages of any desired sizes can be roughly calculated. These values, presented below for a 400 mil x 500 mil package and a 350 mil x 550 mil package, underscore several conclusions:

a. For high performance components, it is extremely desirable to have uniform electrical behavior of all LCCC contact leads, either uniformly good, or even uniformly bad. Otherwise, it is very difficult to CAD a design properly for maximum performance since each pin behaves differently and affects its logic strings differently.

b. Because of "a" immediately above, a square package is more uniform, and even it is not perfect because its corner pads will be roughly $\sqrt{2}$ worse electrically than center pads (a round package would be most uniform, but difficult to use on a circuit board).

c. Rectangular packages are less electrically uniform than square packages; the larger the aspect ratio of the package the worse the nonuniformity from pin to pin.

d. Long aspect ratio packages are not as electrically uniform as are short aspect ratio packages.

The roughly computed comparisons for a 350 mil x 550 mil (long aspect ratio) package and for a 400 mil x 500 mil (short aspect ratio) package at a fundamental frequency of 500 MHz are listed in Table 1.

Short Aspect Ratio Package	Side:	Center Pin Short	Center Pin Long	Corner Pin Short	Corner Pin Long	Uni
Length		250	200	291.5	282.8	mil
Series Inductance		2.5	2.0	2.91	2.83	nH
Series Impedance		7.85	6.28*	9.14*	8.89	Ohm
Shunt Capacitance		.75	.60	.874	.848	pF
Shunt Impedance		424.4	530.5+	363.9+	375.2	Ohm

* Largest Inductive Reactance Ratio at 500 MHz: 1.45:1

+ Largest Capacitive Reactance Ratio at 500 MHz: 1.45:1

Long Aspect Radio Package	Side:	Center Pin Short	Center Pin Long	Corner Pin Short	Corner Pin Long	Uni
Length		275	175	292.6	285.0	mil
Series Inductance		2.75	1.75	2.93	2.85	nH
Series Impedance		8.64	5.50*	9.20*	8.95	Ohm
Shunt Capacitance		.83	.53	.88	.86	pF
Shunt Impedance		385.8	606.3+	362.6+	372.3	Ohm

* Largest Inductive Reactance Ratio at 500 MHz: 1.67:1

+ Largest Capacitive Reactance Ratio at 500 MHz: 1.67:1

Electrical Comparisons Of Two Designs For A 28-Pad Leadless Chip Carr

Table 1

The long aspect ratio package leaves less room in its narrow dimension on the back surface of the chip carrier for installation of decoupling capacitors, particularly if a heat spreader and/or heat stud are also present. Installation of both a heat stud and decoupling capacitors are feasible on the back of the short aspect ratio LCCC.

Thermal Comparisons Between 350 x 550 mil LCCC and 400 x 500 mil LCCC

1. A long aspect ratio heat spreader cannot be as favorable as a shorter aspect ratio spreader, since the lateral thermal conductivity of alumina is low; as a result, the long ends of the heat spreader will not dissipate heat efficiently.

2. Bonded heat sinks on the back of the long aspect ratio package would have to have a smaller diameter (if round heat sinks, the least expensive, are employed) by 50 mils for the long aspect ratio package than they would for the short aspect ratio package. To regain efficiency, heat sinks with rectangular cross section would be required, and these are nearly prohibitively costly.

$$P_D = \frac{T_J - T_A}{\theta J_C + \theta C_S + \theta S_H + \theta H_A}$$

From Thermalloy Catalog
80 HS-7, Page 6

P_D - Watts Being Dissipated
T_J - Die Junction Temp in °C
T_A - Ambient Temp in °C
θ_{JC} - Junction to Ceramic Thermal Resistance in °C/Watt
θ_{CS} - Ceramic to Surface Thermal Resistance in °C/Watt
θ_{SH} - Surface to Heat Sink Thermal Resistance in °C/Watt (Copper Shank)
θ_{HA} - Heat Sink to Ambient Thermal Resistance in °C/Watt

Max Die Temp = 150°C for ECL Logic (T_J) — From ECL Data Book, 1977, pp 6-13
Max P_D = 1.3 Watts (-4.5 Volts x -.283A: 100136 CNTR) — From ECL Data Book, 1977, pp 10-30
Max T_A = 25 °C (77F Maximum in Lab)
θ_{JC} = 15-17 °C/Watt (Eutectic Solder Die Attach) — From Fairchild Engineering Dept.
θ_{CS} = 2.6 °C/Watt (See Calculations Below) — Calculated From Kyocera Catalog, 3T8009TD
θ_{SH} - 2.2 °C/Watt (See Calculations Below) — Calculated From Reference Data for Radio Engineers
θ_{HA} = 9-21 °C/Watt (See Calculations Below) — From Wakefield and Thermalloy

$P_D \times \theta_{JA} = T_J - T_A$
Thus:
$T_J = (P_D \times \theta_{JA}) + T_A$
$\theta_{JA} = 17 + 2.6 + 2.2 + 21 = 42.8$ °C/Watt x 1.3 Watts = 55.64 °C + 25 °C = 80.6 °C Junction for 100136 Chip in Lab Air With Fans

Actual Temperature Should be Less Since Heat Flow Will Occur to the Sides, Into the Board, and will Radiate from the Top Surface Not Occupied by the Heat Sink

CHIP CARRIER THERMAL INFORMATION

Table 2

θ_{JC} DATA: 400 x 400 mil Chip, Solder Die Attach, 20 mil Thick of Al_2O_3 - θ_{JC} = 17 °C/Watt, θ_{JA} = 73 °C/Watt in Still Air
450 x 450 mil Chip, Solder Die Attach, 20 mil Thick of Al_2O_3 - θ_{JC} = 15 °C/Watt, θ_{JA} = 60 °C/Watt in Still Air
Thus Our 400 x 500 mil Package θ_{JA} Will Be Approximately Equal to the 450 x 450 mil Chip, Even Taking Into Account a 25 Mil Thick Layer Instead of Just 20 Mils (Solder Joint Dominant; (From Engineering Department, Fairchild)

θ_{CS} DATA: A-440 Alumina Thermal Conductivity @ 20°C = (.04 Cal) (Cm)/Cm^2) (Sec) (°C)
Heat Sink Area for Small Cavity = 175 Mil Diameter, Thus R = .22 cm Area = .15 cm^2
Heat Path Through Al_2O_3 = 25 Mils Thick = .065 Cm Thick

(Since 1 Cal/Sec = 4.186 Watts) C = Conductivity R = Resistance (1/C=R)

$$.04 \frac{(Cal)\ (Cm)}{(Cm^2)\ (Sec)\ (°C)} \times \frac{.15\ Cm^2}{.065\ Cm} = .092 \frac{Cal}{(Sec)\ (°C)}$$; .092 x 4.186 = .39 Watts/°C = 2.6°C/Watt

θ_{SH} DATA: Al: .48 Cal Cm/(Cm^2) (Sec C) or 2.18 Watts/(Cm) (°C)
Cu: .91 Cal Cm/(Cm^2) (Sec C) or 3.94 Watts/(Cm) (°C)

Copper Thermal Conductivity = 3.94 Watts/(Cm) (°C) = (3.94 Watts) (Cm)/(Cm^2) (°C)

$$3.94 \frac{(Watts)\ (Cm)}{(Cm^2)\ (°C)} \times \frac{.15\ Cm^2}{(1.27\ Cm)} = .465 \text{ Watts/°C} = 2.2°C/Watt$$
Conductivity Resistance

An Al Shank Would Raise Junction Temp an Additional 2°C.
Thermal Conducitivity of 62/38/2 Solder = .31 Watts/(Cm) (°C)
THUS:

$$\frac{(.31\ Watts)\ (Cm)}{(Cm^2\ (°C)} \times \frac{.15\ Cm^2}{(.0078\ Cm)} = 5.96 \text{ Watts/°C} = .167 \text{ C/Watt}$$ (.0078 Cm of solder 3 mils insignificant

CHIP CARRIER THERMAL INFORMATION

θ_{HA} DATA: Dependent Upon Air Flow Rate.

		(0 MPH) No Flow	(1.1 MPH) 100 ft/min	(4.5 MPH) 400 ft/min
For Wakefield #'s	202 B	75 °C @ 1 Watt	60 °C/Watt	21 °C/Watt
	222 CB	55 °C @ 1 Watt	28 °C/Watt	9 °C/Watt
Thermalloy #'s	2224 B	85 °C @ 1 Watt	65 °C/Watt	35 °C/Watt

Characteristics of Mayo-Designed 28-Pad LCCC

As a result of these analyses, the Mayo design for a 28-pad LCCC was accepted by the Fairchild engineers. Figures 28 and 29, artists conceptions of the 28-pad LCCC design, are similar to Figures 25 and 26 in the Year Two Year-End Report, but reflect the changes in pin count, edge dimensions, and die well cavity sizes in the new design. Figure 28 depicts the cavity side and the back surface views of the 28-pad leadless ceramic chip carrier. As in the 32-pad design, provision has been made to employ a recessed lid by using a four-layered structure to allow the silicon die to be mounted on the circuit board in the lid-down configuration.

As depicted in Figure 29, the first layer supports the die-attach surface; the second layer contains the signal pin leadouts and provides the attachment points along the edge of the die well for the wire bonds to the die; the package was also established to reduce series inductance by using the newer bonding method referred to as Beam Lead bonding. The third layer of the chip carrier is the spacer layer, which provides a shelf for the lid and seal ring onto which a small Kovar or ceramic lid can be recess mounted.

Lastly, the uppermost or fourth layer of the chip carrier supports a number of small tungsten bumps which are extensions of the signal traces on the second layer of the chip carrier. The

AIR-COOLED LEADLESS CERAMIC CHIP CARRIER FOR HIGH POWER, HIGH FREQUENCY DIGITAL INTEGRATED CIRCUITS
(28 Pads; Two Die Cavity Versions; Recessed Lid For Mounting Die Well Down; 94% Alumina Substrate)

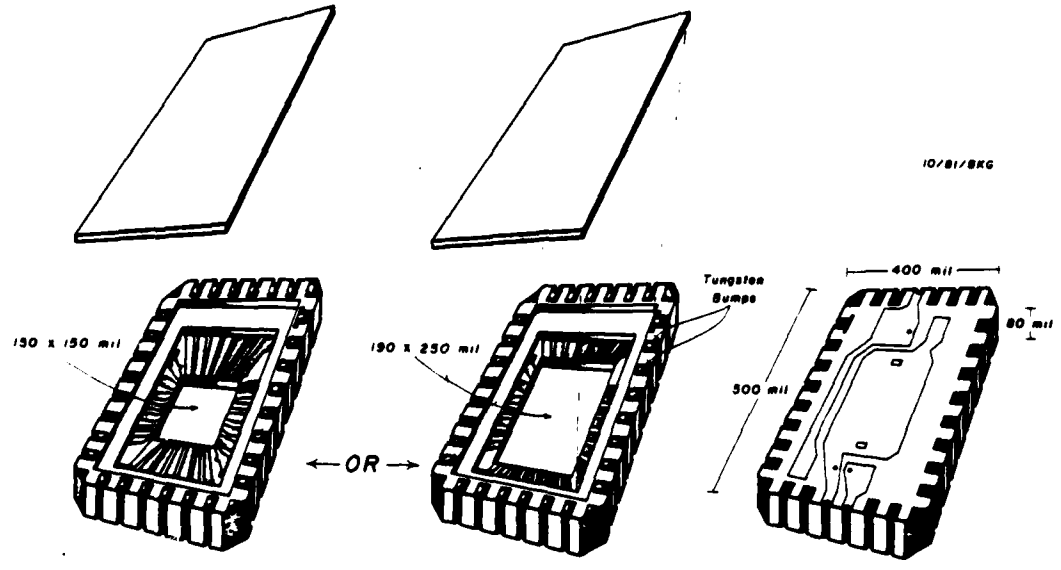


FIGURE 28

artist's conception of Figure 28 illustrates these tungsten bumps. The bumps are approximately 5 mils in height, 30 mils in length and approximately 20 mils in width, and serve two basic functions in the Mayo-designed chip carrier. First, manufacturing tolerances could create a situation in which the Kovar lid is not recessed adequately and might protrude one to two mils

above the surface of the chip carrier. The 5 mil tungsten bumps will allow the chip carrier to be surface mounted in the lid-down configuration whether or not a perfect recessed lid arrangement is achieved in every chip carrier. Second, these bumps will serve as solder attachment points for vapor phase reflow solder

AIR-COOLED LEADLESS CERAMIC CHIP CARRIER
FOR HIGH POWER, HIGH FREQUENCY
DIGITAL INTEGRATED CIRCUITS
(28 Pads, Two Die Cavity Versions ;
Recessed Lid for Mounting Die Well Down ;
94% Alumina Substrate)

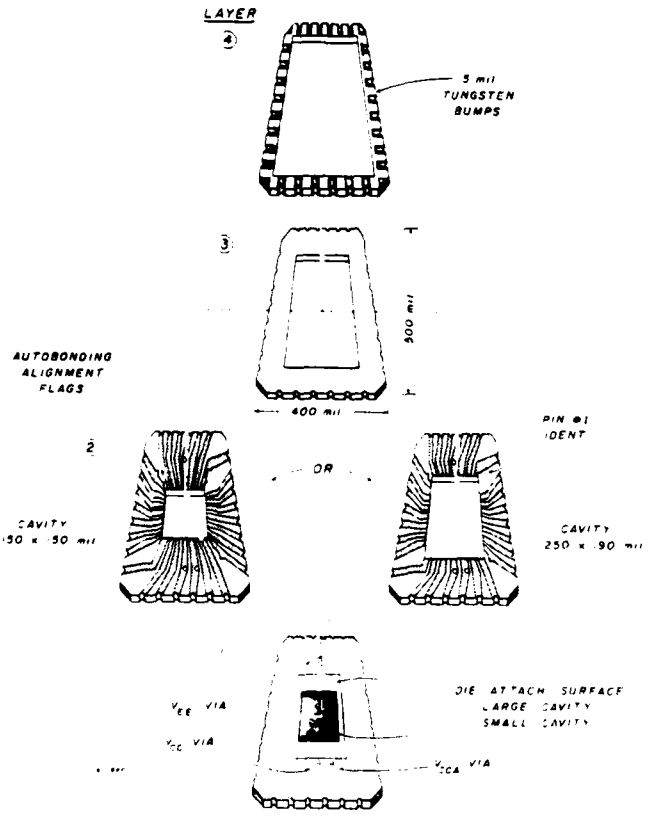


FIGURE 29

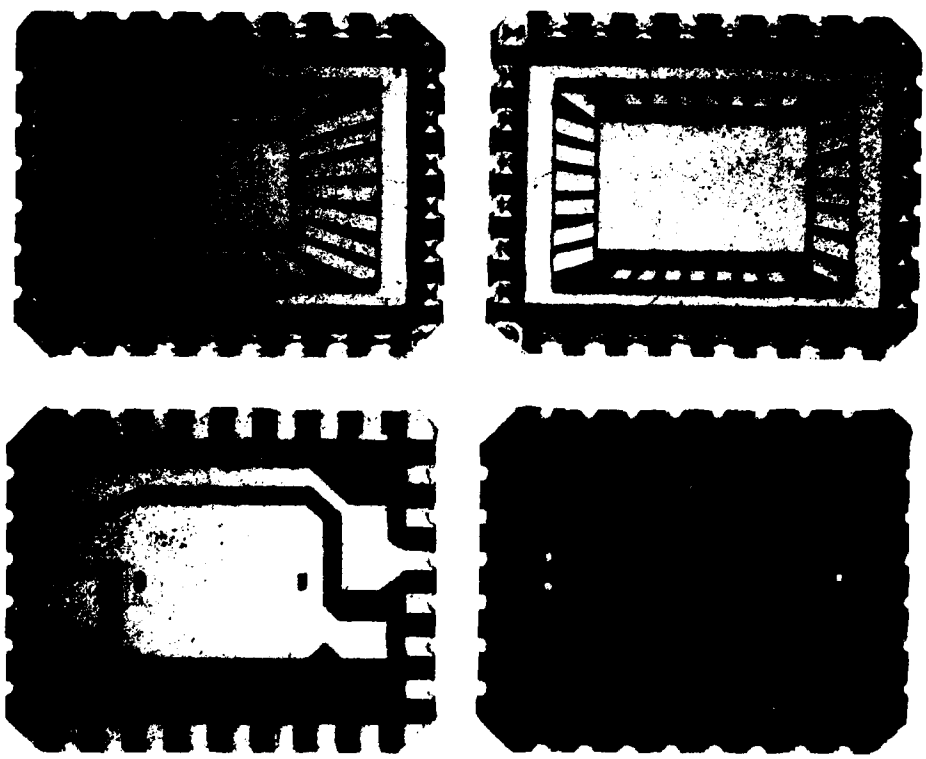
bonding of the carriers to a circuit board, and will also provide for the creation of small columns of solder between the tungsten bump and the circuit board. The existence of these malleable masses of solder should allow some thermal expansion strain relief between the board foils and the leadless chip carrier itself, thereby tending to reduce solder bond breakage as the chips and boards undergo thermal cycling.

Although the 28-pad leadless chip carrier of Figures 28 and 29 was designed for inverted mounting, provisions were made in the first production run of these devices for lid-up mounting as well; note that the edge castellations extend from one surface of the chip carrier to the other and can be plated along their entire length, since there would be no possibility of short circuits to the recessed Kovar lid. In its initial configuration, the chip carrier could thus be solder mounted to a printed circuit board in a lid-up configuration using fillet solder joints.

Figure 28 also includes a modified heat spreader and attachment points for decoupling capacitors on the back surface of the chip carrier; although the Mayo group considers this heat spreader and decoupling design to be quite nonoptimum, the layout depicted in this figure was intended to accommodate several constraints placed upon the heat spreader design by the Fairchild group. Although the first production run of leadless chip

carriers employed this heat spreader design, Fairchild has subsequently removed its constraints, and the Mayo group has redesigned the heat spreader. Future production runs will use the modified heat spreader design, which should be considerably more efficient.

The design features included to improve the electrical performance of the Mayo-designed leadless ceramic chip carrier may also be observed in Figure 30. The rightmost panel of this Figure depicts the back surface of the chip carrier, including the heat spreader and attachment for a soldered heat stud. The corners of the chip carrier are chamfered at a 45° angle and are metallized and castellated for solder connection to ground plane contacts on the printed circuit board; a tungsten bump is also positioned at each of the four corners for the same purpose. Connection of the back metallization and the soldered heat stud to ground allows these structures to serve as an electrical shield for the ECL die; the back metal also provides an additional decoupling capacitance of approximately 100 pF between die attach metallization (which for ECL components is connected to the -4.5 volt bus) and ground. At the high operating frequencies of subnanosecond ECL, a 100 pF capacitance provides a nontrivial decoupling effect to minimize V_{EE} voltage transients observed by the ECL die.



FIRST PRODUCTION RUN OF MAYO-DESIGNED 28-PAD LEADLESS CHIP CARRIERS. TWO DIE CAVITY VERSIONS ARE SHOWN, WITH BACK-SIDE HEAT SPREADER VERSION AND HEAT SPREADER-FREE VERSION ALSO DEPICTED.

FIGURE 30

Conversely, the back surface metallization may increase the parasitic input shunt capacitance of the signal leads; this increased shunt capacitance has been calculated to be less than .1 pF, a acceptable level if correct.

As described earlier, the back surface of the chip carrier also supports two small rectangular metallized areas electrically connected to two center castellations on one edge of the chip carrier; these two castellations are the ground supply pads for the chip carrier. A third rectangular area connecting to a single edge castellation is attached to the -4.5 volt feed. Figure 29, an exploded view of all four layers of the chip carrier, displays small solid vias connecting these rectangular metallization areas to the internal ground and -4.5 volt bus leads on Layer 2. The ground runs from the metallized rectangular patches are attachment points for small 4700 pF NPO chip capacitors, which can be soldered on the back of the chip carrier to further decouple the -4.5 volt die attach plane to ground.

Figure 29 also indicates two additional features intended to improve the electrical performance of the chip carriers. First, no electroplating fingers between the signal leads are evident on Layer 2. Note also that the gold-plated die attach area on Layer 1 of the chip carrier supports only a single electroplating finger 10 mils in width extending to the edge of the chip carrier. The single electroplating finger on Layer 1 is positioned under the V_{CC} ground feed, and hence will cause the minimum possible disturbance of the characteristics of adjacent signal leads. The residual slight degradation will have to be tolerated.

Note that for a given die well area, a leadless chip carrier employing a recessed lid for lid-down mounting must always be larger than the equivalent chip carrier using a surface mounted Kovar lid, since the recessed lid requires a mounting recess and lid seal ring which increases the edge dimensions of the chip carrier by approximately 100 mils in length and width, and approximately 10-15 mils in thickness.

This single chip carrier footprint is acceptable for components from a few thousand mil^2 area, such as the F100102 five section OR-gate, to the largest memory parts now planned, 64K x 1 and 16K x 4 memory components of greater than 30,000 mil^2 area. However, for packaged components to pass shock and vibration testing, the wire bonds between the pads on the ECL dice and the bonding attachment points on the leadless chip carrier must be within a critical range of lengths, i.e., not less than 30 mils nor greater than 100 mils. If only a single cavity size were used, the length of the bonding wires required for the smallest ECL dice would be too great. To alleviate this problem while maintaining the capability for maximum die size in this footprint, Figure 29 shows that Layer 2, which creates the boundary of the die well cavity and supports the bond wire attachment points of the chip carrier, has been manufactured in two versions, one of which will accommodate small ECL dice of a few thousand mil^2 area, and a second pattern which defines a larger die well cavity for large components. Since the other

three layers of the chip carrier are unaffected by the alternate versions of the Layer 2, the additional cost to manufacture two alternate versions is acceptable.

Although there may be a slight degradation in electrical performance for the smallest die sizes due to the extra lengths of signal leads on Layer 2 of the chip carrier, this additional length never exceeds 50 mils for any lead, equivalent to approximately .5 nH of series inductance and a fraction of a pF of shunt capacitance; the propagation delay increments will be on the order of 2.5 psec. These performance degradations will be tolerated to achieve standardization on a single leadless chip carrier accepting a wide variety of part types. Feasible bondout patterns have been identified for all presently available or currently envisioned subnanosecond ECL memory, logic, and arithmetic parts if encapsulated in this new LCCC.

Also incorporated in the design of this package are several advantageous mechanical features. As described earlier, the solder columns which form under the tungsten bumps may to some extent dissipate the stresses on the chip carrier which would occur if the carriers were flush mounted and fillet soldered at their castellations to the printed circuit cards. In addition, the tungsten bumps will elevate the chip carrier above the surface of the board by 4-6 mils, thereby allowing flux solvents to remove the mildly activated fluxes from the interstices between the chip carrier and the circuit board. Complete flux removal

should reduce slow corrosion of the surface conductors on the logic board. Lastly, Figures 28 and 29 indicate four triangular patterns in the interior corners of the second layer of the chip carrier. These triangular structures were included in the design to allow modern optically registered autobonders to bond die installed in this package.

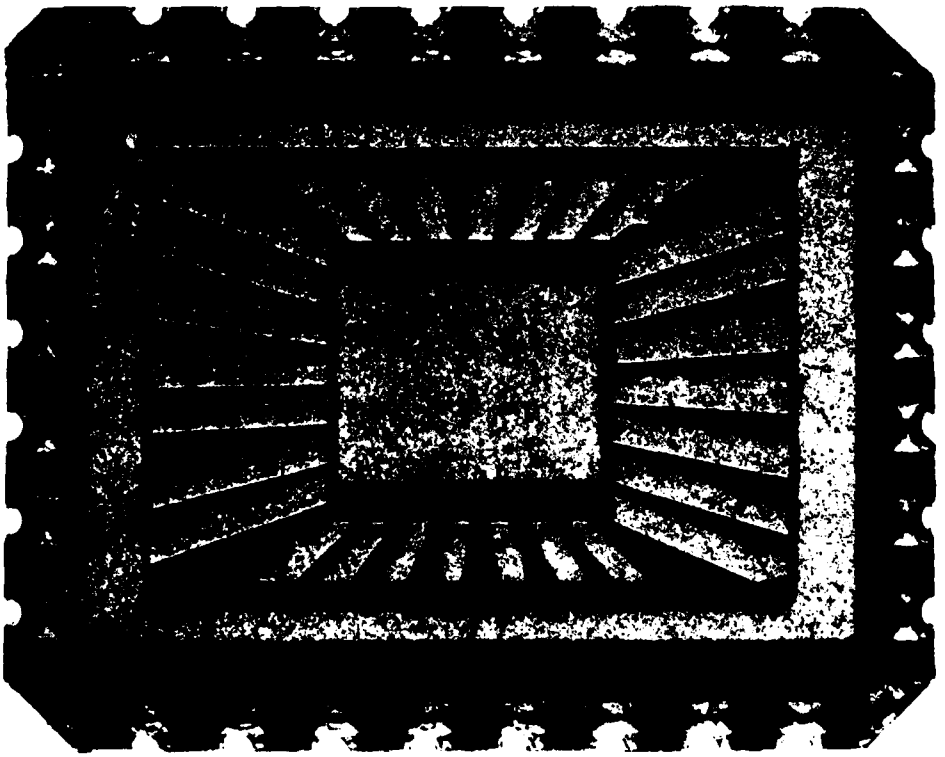
First Production Run of Mayo LCCCs and Measurement Results

Following negotiation with Fairchild Camera and Instrument Corporation and with Kyoto Ceramics International, a hard tool was manufactured, and a preliminary production run of both die well sizes of the 28-pad leadless chip carriers was carried out. Figure 30 depicts both cavity size versions, i.e., the 150 mil x 150 mil die cavity, and the 190 mil x mil die cavity. The lower left chip carrier depicts the back metallization employed on both carriers. For purposes of electrical tests, the vendor manufactured a small quantity of both leadless chip carrier versions without the back metallization, as may be observed in the lower right portion of Figure 30. Note the three small circular dots on the back of the carrier, which are the decoupling vias which penetrate the back surface of the LCCC and make contact with the V_{EE}, V_{CC} and V_{CCA} leadin fingers.

Figure 31 shows an enlarged photomicrograph of the small die-cavity leadless chip carrier. Note that the signal traces are considerably wider in actuality than in the artist's conception of Figure 29. The Kyoto Ceramics engineers modified our specifications to minimize overall DC resistance of the bonding fingers by widening each trace, thereby increasing the intertrace shunt capacitance. A "smearing" of the gold metallization around the tungsten bumps, and misalignment of the gold metallizations with respect to the castellation cuts on the edge of the chip carrier, were also detected. Lastly, at the four chamfered corners of the chip carrier, smearing of the gold metallization was detected at the extremes of the chamfer in the direction of the next adjacent pads (see also Figure 32).

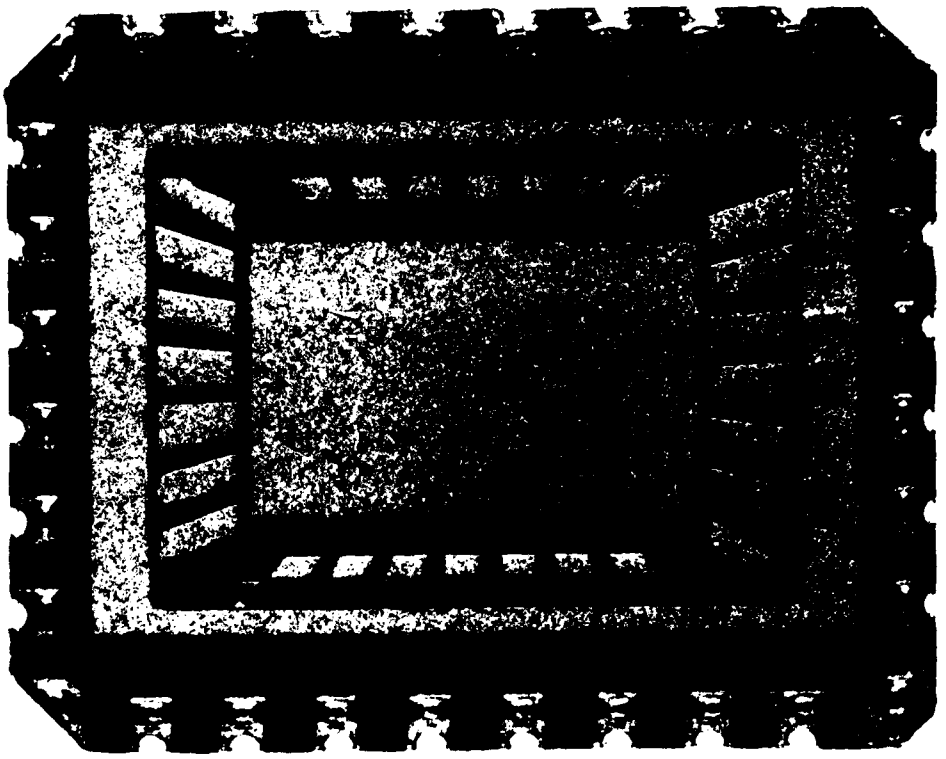
Figure 33, a photomicrograph of the back surface of the chip carrier, shows evidence of registration alignment deficiencies between the artwork layers and the castellation punch tool. Figure 34, a photomicrograph of the edge of the large-cavity version of the leadless chip carrier, clearly shows the smearing of the gold contact surfaces in the vicinity of the tungsten bumps. The most serious smearing occurred in the region of the edge contact tungsten bumps; the dimension of the unmetallized guard band between each contact and the edge of the lid cavity was reduced by the gold smearing from 5 mils to 2 mils. We were concerned that the minimum clearance between the metallized tungsten contact bumps and the recessed Kovar lid might provide an insufficient barrier to the formation of solder whiskers between the

signal contacts and the lid, causing short circuits. The correction for the problem, described in greater detail below, could be either a reduction in the nominal length of these contact pads or an increase in the thickness of Ceramic Layer 4 to assure a greater vertical separation between the outer surface of the Kovar lid and the surface carrying the tungsten bumps.



PHOTOMICROGRAPH OF SMALL CAVITY VERSION OF LCCC. CONDUCTING TRACES ARE UNNECESSARILY WIDE IN THESE FIRST PRODUCTION COMPONENTS.

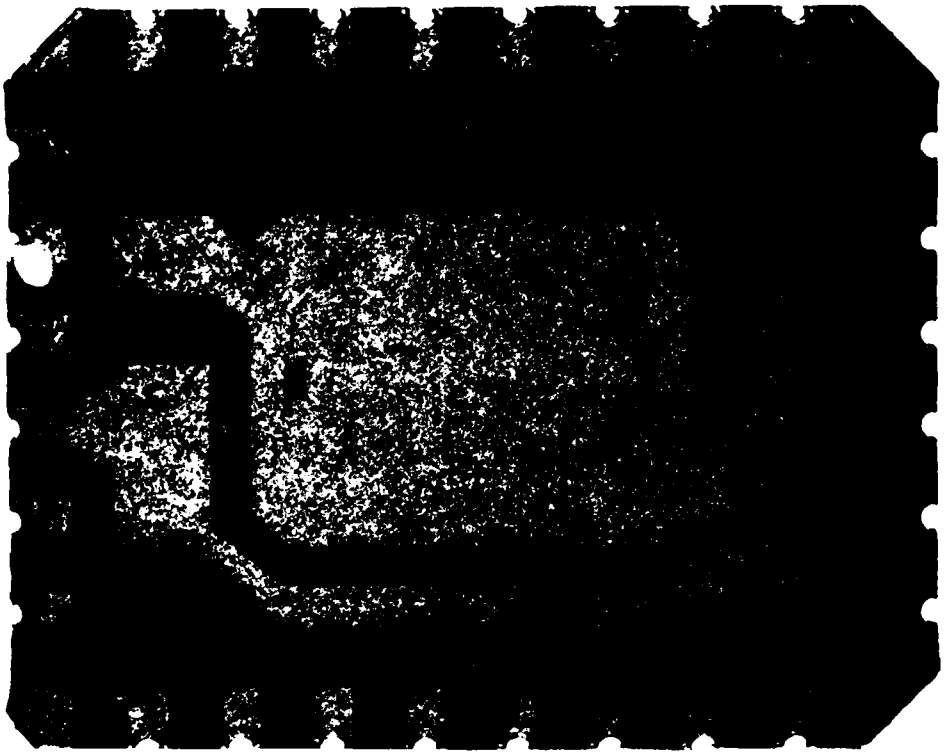
FIGURE 31



PHOTOMICROGRAPH OF LARGE CAVITY VERSION OF LCCC. THIS VERSION ALSO EXHIBITS UNNECESSARILY WIDE CONDUCTING TRACES. NOTE GOLD SMEARING ON CHAMFERED CORNERS.

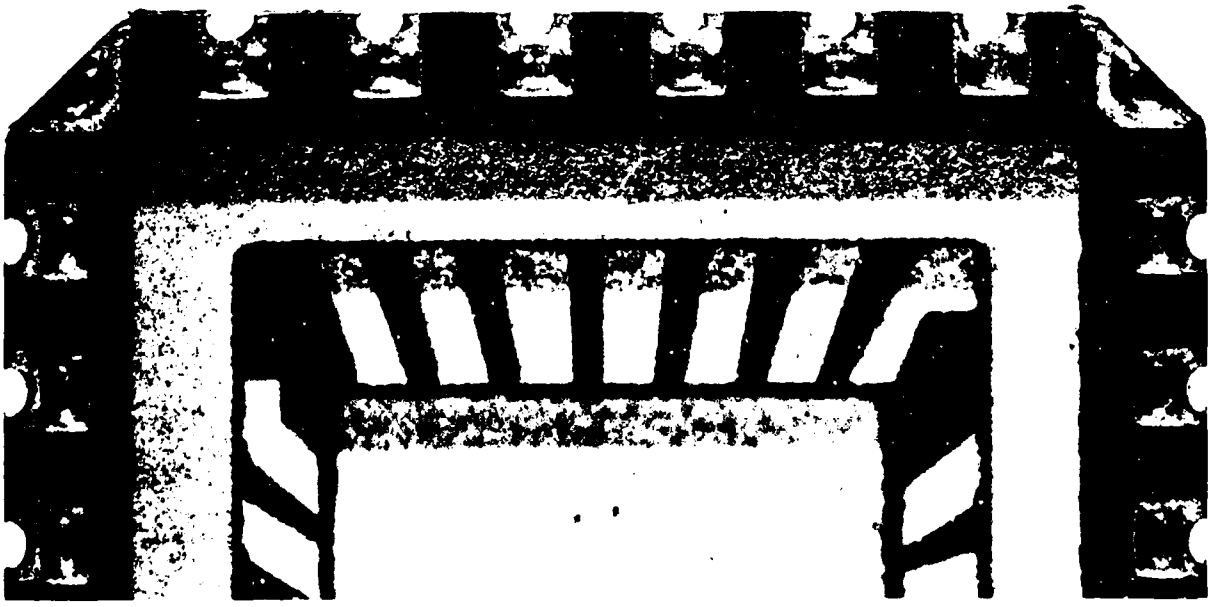
FIGURE 32

Figure 35 is a photomicrograph of the edge of the small cavity version of the leadless chip carrier, showing the tungsten bumps, the castellations which completely traverse the thickness of the chip carrier, and the metallized chamfered corners. These castellations allow the formation of complete solder fillet



PHOTOMICROGRAPH OF BACK SURFACE OF FIRST PRODUCTION RUN OF THE MAYO-DESIGNED LCCC. INEFFICIENT HEAT SPREADER, PICTURED HERE, HAS BEEN REDESIGNED.

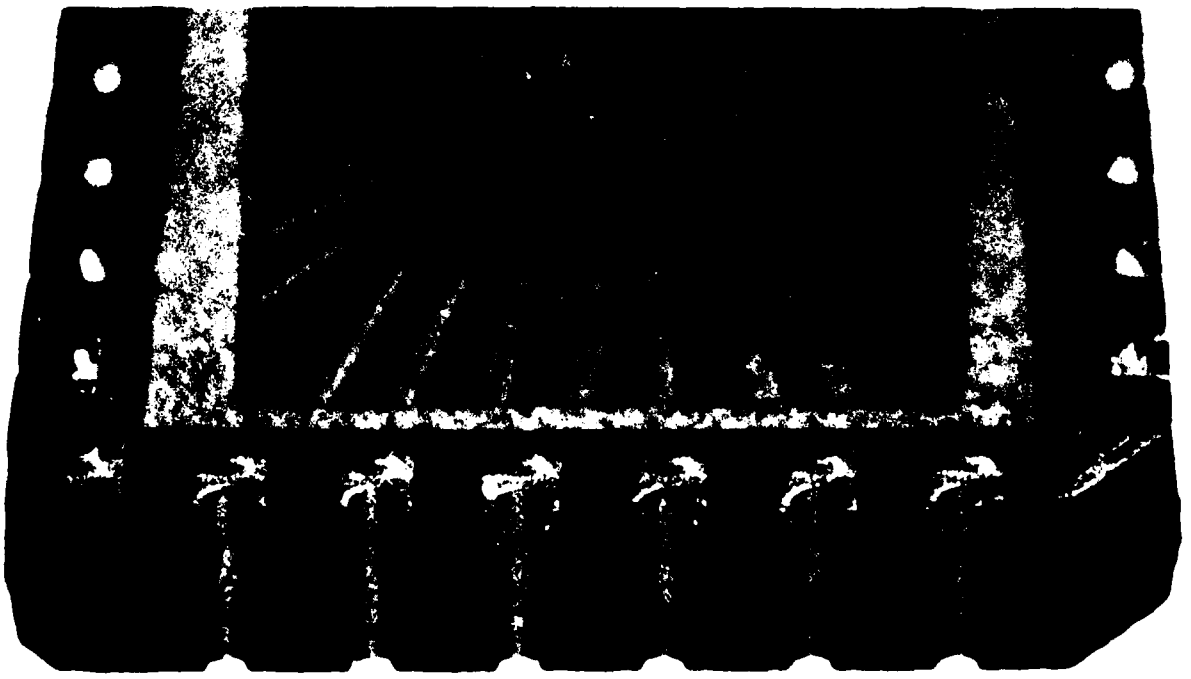
FIGURE 33



PHOTOMICROGRAPH OF 5 MIL TUNGSTEN STANDOFF BUMPS ON LID SIDE OF LCCC. NOTE GOLD SMEARING ON CHAMFERED CORNERS AND MISALIGNMENT BETWEEN CONTACT PADS AND CASTELLATIONS.

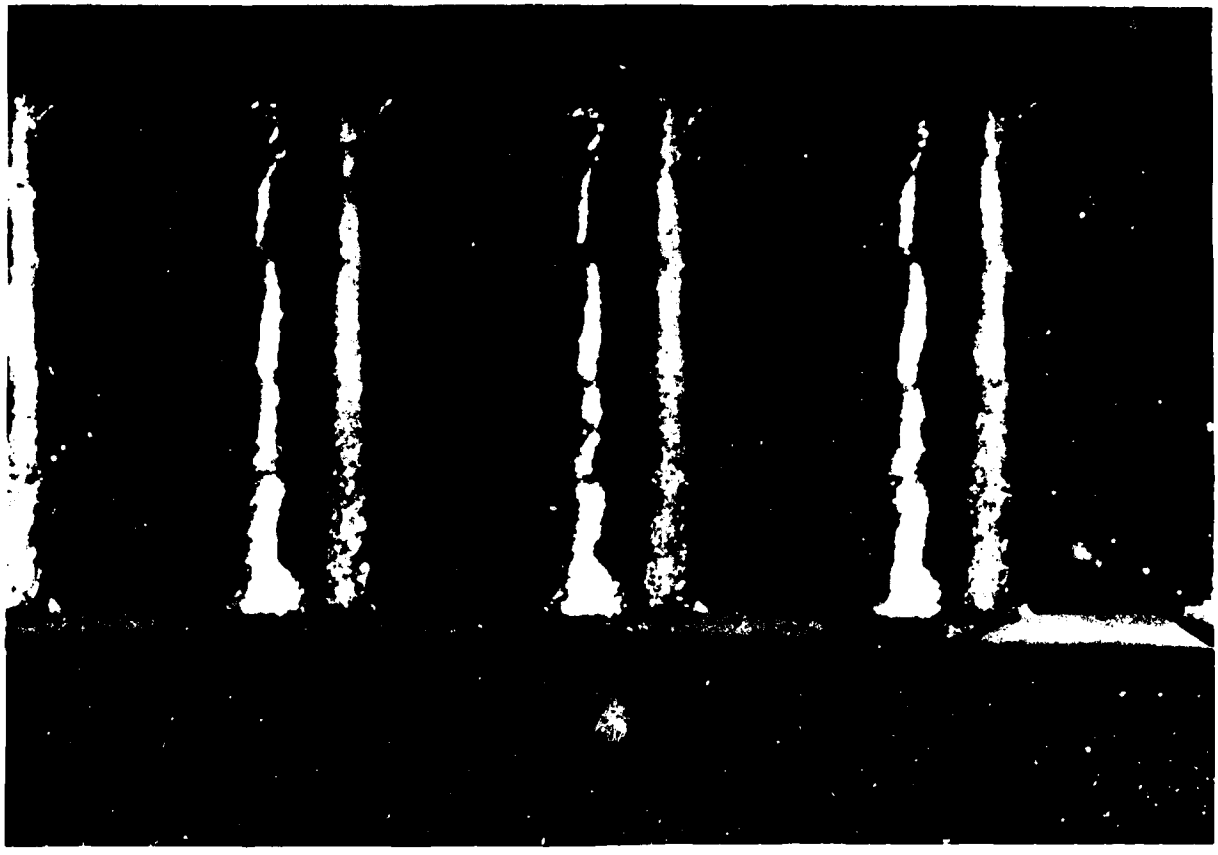
FIGURE 34

joints, and also allow mounting in either the lid-up or the lid-down configuration. Smearing of the gold plating on the right-most chamfered corner is evident in these photographs. The vendor has agreed to improve the dimensional tolerances on the plating metallization step to alleviate this problem.



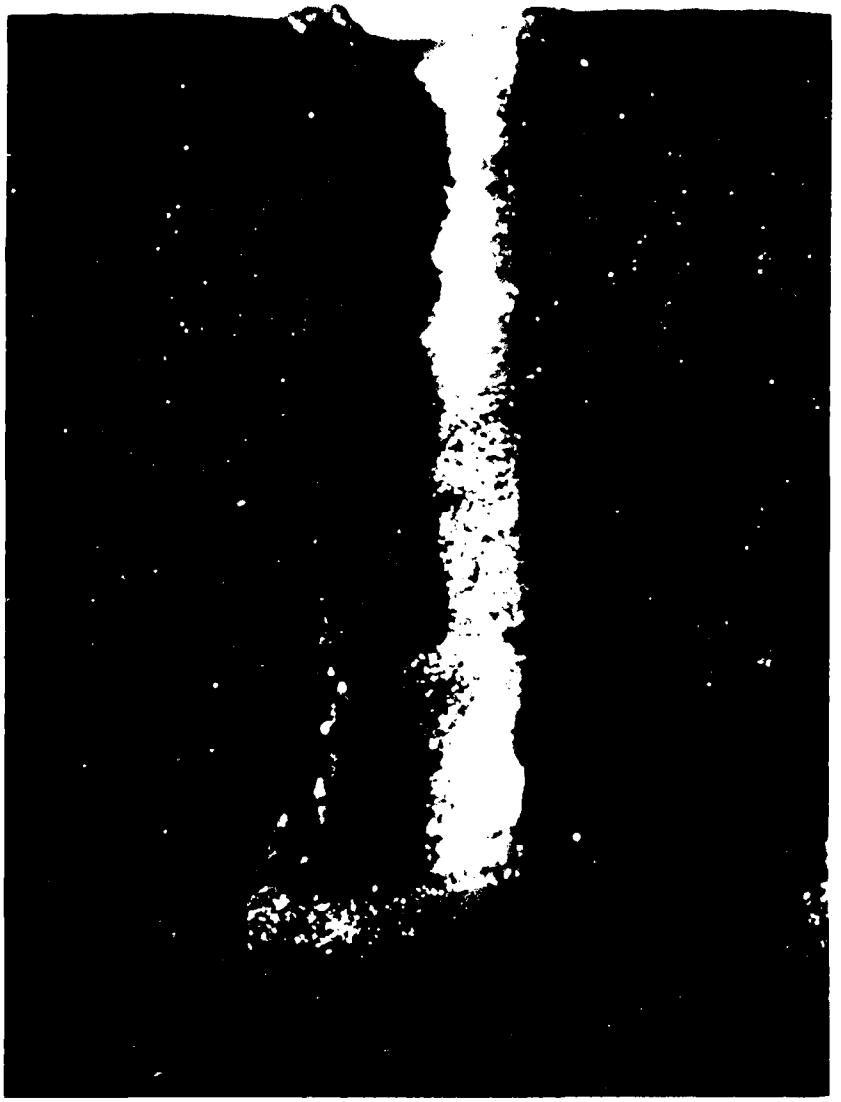
EDGE VIEW OF TUNGSTEN BUMPS, CONTACT PADS, AND CASTELLATIONS OF MAYO-DESIGNED LCCC. CASTELLATIONS PENETRATE THE ENTIRE THICKNESS OF STRUCTURE.

FIGURE 35



EDGE VIEW OF MAYO-DESIGNED LCCC SHOWING THE MOUNTING POSITION OF THE STRUCTURE, AND THE STANDOFF EFFECT ACHIEVED BY TUNGSTEN BUMPS

FIGURE 36

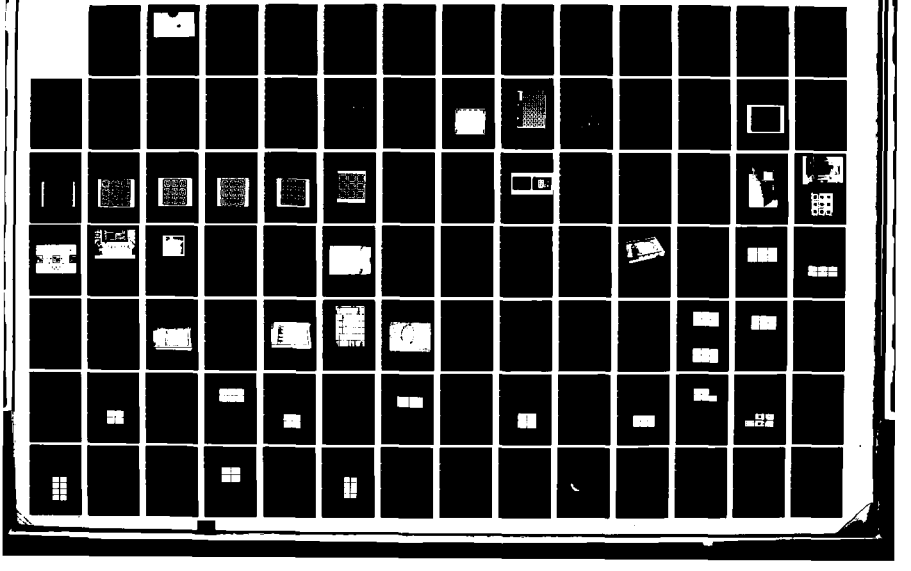


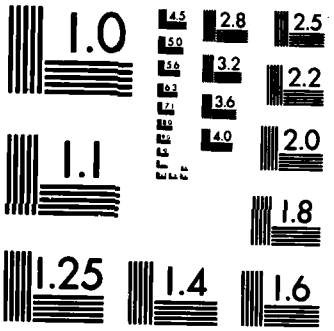
PHOTOMICROGRAPH OF GOLD PLATED CASTELLATION AT THE EDGE OF THE LCCC. TUNGSTEN BUMP IS AT THE BOTTOM OF THE CHANNEL.

FIGURE 37

AD-A126 156 LEADLESS CHIP CARRIER PACKAGING AND CAD/CAM (COMPUTER-AIDED DESIGN/COMPUT.. (U) MAYO CLINIC ROCHESTER MN SPECIAL PURPOSE PROCESSOR DEVELOPMEN.. 2/3

UNCLASSIFIED B K GILBERT DEC 82 AFWAL-TR-82-1159 F/G 9/1 NL





VIEW OF LCCC CONTACT PAD AND ASSOCIATED TUNGSTEN BUMP. NOTE LEACHING OF GOLD SURFACE WHICH OCCURRED DURING TUNGSTEN APPLICATION.

FIGURE 38

Figure 36 is a cross section photomicrograph of a Mayo LCCC placed on a horizontal surface as it would be on a circuit board. The LCCC was back-lighted to show the spacing effect provided by the tungsten bumps, which allow the free flow of flux cleaning agents. Figure 37 is a photomicrograph of one of the edge castellations; the uneven edges of the castellations are the outlines of the individual ceramic layers which compose the chip

carrier. Figure 38 is a photomicrograph of one of the tungsten bumps and its associated metal pad and castellation; note the uneven surface texture of the gold contact pad, which is apparently caused by the inadvertent leaching of gold during the process of electroplating the tungsten bumps. The castellation is misaligned with the gold contact pad, a fabrication problem which Kyoto Ceramics has agreed to attempt to remedy. The small gold lip on the lower edge of the tungsten bump extends approximately 3 mils closer toward the bottom of the photograph than originally intended in the design. Unfortunately, this bleeding of the gold minimizes the width of the solder guard band between the contact and the Kovar lid.

Electrical Characteristics Of Mayo-Designed Leadless Chip Carriers

Electrical measurements were performed on the first production run of 28-pad leadless ceramic chip carriers, the results of which are presented in Figures 39, through 45. Figures 39 and 40 display the lead series inductance measurements from the small and large die-cavity versions of the chip carrier respectively; in each figure, a small cartoon indicates the contacts which were used in these measurements. Because of the layout characteristics of the chip carriers, contact "A" is the longest run, with successively shorter signal path lengths for contacts "B", "C", and "D", respectively. These decreasing lengths are mirrored

by the decreasing series resistance of the successive contacts, from 89 milliohms to 66 milliohms in the case of the small cavity device, and from 59 milliohms to 37 milliohms respectively for the large cavity device (the smaller cavity version has longer signal runs, and vice versa).

The lead series inductance ranges from 3.5 nH for contact "A" to 2.5 nH for contact "D" in the small cavity version of the chip carrier, and from 2.7 nH for contact "A" to 2.0 nH for contact "D" in the large die-cavity version. These values are somewhat larger than for the best of the commercial leadless chip carriers, and larger than we would like; nonetheless, these series inductance values are the second best that we have seen in all of the measurements made to date on various forms of encapsulation. Fortunately, there are feasible methods of decreasing the series inductance almost to zero, and their investigation will form a major portion of the work designated for the coming year.

Somewhat more disturbing and unexpected results were discovered in an analysis of the separate parasitic shunt capacitances associated with these packages, which resulted in immediate changes to the chip carrier design, the hard tooling, and to the next production run of devices. Figures 41 and 42 depict the interlead shunt capacitances for the small and large cavity versions of the chip carrier respectively. Because the small cavity version exhibits longer traces, its shunt capacitances are

somewhat higher than for the larger cavity version. As described earlier, a propagating signal is exposed to twice the intertrace shunt capacitance presented on these charts; for example, in Figure 41, contact "B" would observe about 1.5 pF shunt capacitance. These values are higher than originally estimated, in part because the vendor fabricated the signal traces as wide as possible to minimize DC resistance, but thereby decreased the width of the non-conducting guard band between adjacent traces.

ELECTRICAL CHARACTERISTICS OF MAYO-DESIGNED 28 CONTACT LEADLESS CERAMIC CHIP CARRIER FOR HIGH FREQUENCY, HIGH POWER CIRCUITS
(Version 1, 150 x 150 mil Cavity, Measurements via HP4191A Impedence Analyser)

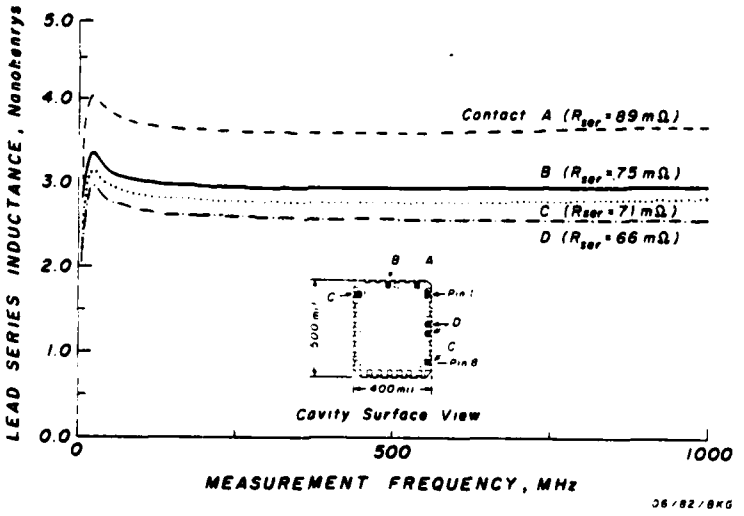


FIGURE 39

An additional source also contributes to the interlead shunt capacitance, through an indirect mechanism. Figure 43 displays the shunt capacitances between the leads of the two die cavity versions and their metallized lid seal rings; these shunt parasitics, ranging from .7 pF to .9 pF, are as large as or larger than the interelectrode shunt capacitances, because of the broad overlay area between the seal ring metallization and the underlying signal contacts. The seal ring metallization also contributes indirectly to the interlead shunt capacitance since a small parasitic capacitor exists between each contact lead and

ELECTRICAL CHARACTERISTICS OF MAYO-DESIGNED 28-CONTACT LEADLESS CERAMIC CHIP CARRIER FOR HIGH FREQUENCY, HIGH POWER CIRCUITS
(Version 1, 190 x 250 mil Cavity; Measurements via HP4191A Impedance Analyzer)

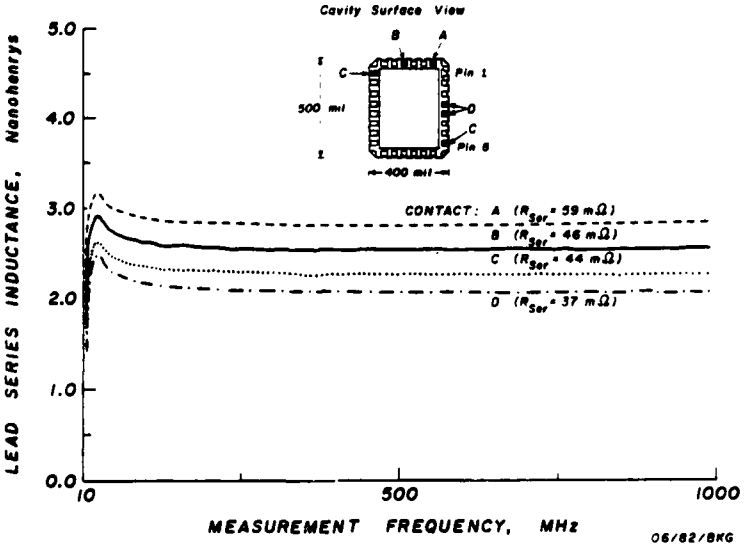


FIGURE 40

ELECTRICAL CHARACTERISTICS OF MAYO-DESIGNED
28-CONTACT LEADLESS CERAMIC CHIP CARRIER FOR
HIGH FREQUENCY, HIGH POWER CIRCUITS
(Version 1, 150 x 150 mil Cavity;
Measurements via HP4191A Impedance Analyzer)

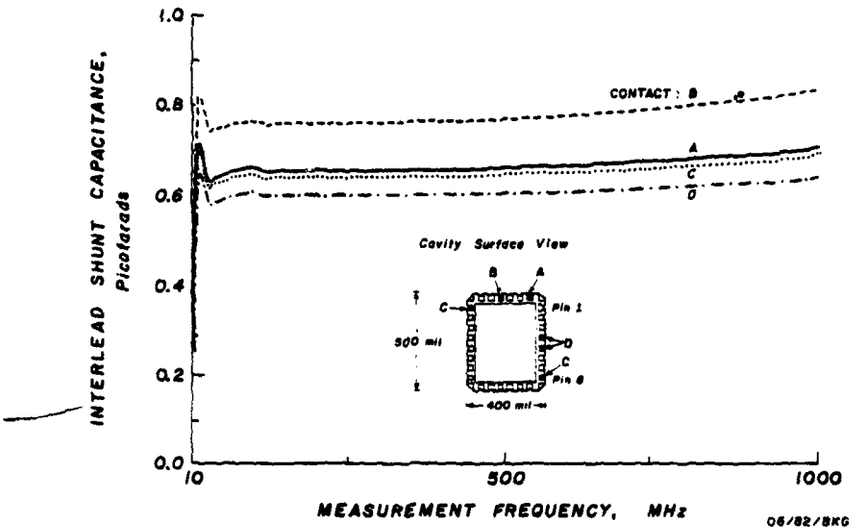


FIGURE 41

ELECTRICAL CHARACTERISTICS OF MAYO-DESIGNED
28 CONTACT LEADLESS CERAMIC CHIP CARRIER
FOR HIGH FREQUENCY, HIGH POWER CIRCUITS
(Version 1, 190 x 250 mil Cavity,
Measurements via HP4191A Impedence Analyser)

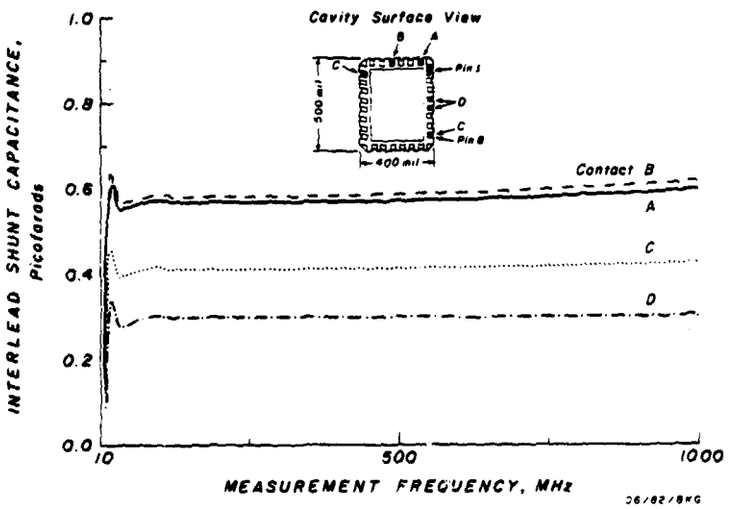


FIGURE 42

ELECTRICAL CHARCTERISTICS OF MAYO-DESIGNED 28-CONTACT LEADLESS CERAMIC CHIP CARRIER FOR HIGH FREQUENCY, HIGH POWER CIRCUITS

(Version 1, 150 x 150 mil and 190 x 250 mil Cavity; Measurements via HP4191A Impedance Analyzer)

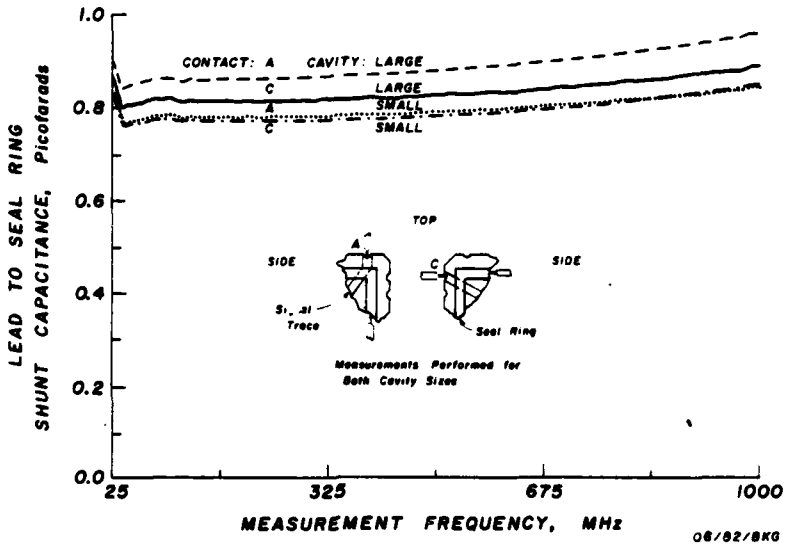


FIGURE 43

the seal ring metallization, and a second parasitic capacitor between the seal ring metallization and the next adjacent contact lead on both sides of the lead in question. The seal ring parasitic capacitance may be the major contributor to the interelectrode capacitances described in the Figures 41 and 42. The shunt parasitics contributed by the seal ring metallization are unacceptably high, and require corrective measures.

Figures 44 and 45 depict the shunt capacitance between the die-attach area and the signal contacts for the two die-well sizes of chip carrier. We believe that this source of parasitic shunt capacitance will also be minimized by the narrowing of the signal traces, but it will be impossible to remove entirely unless the metallized die-attach area is removed entirely. Such a change would no longer permit eutectic solder scrub attachment of the die to the chip carrier, which in turn would require epoxy or polyimide materials in the die-attach process. This change, which would require a major alteration in manufacturing methods, is also under discussion with Kyoto Ceramics and Fairchild Camera and Instrument Corporation.

ELECTRICAL CHARACTERISTICS OF MAYO-DESIGNED 28 CONTACT LEADLESS CERAMIC CHIP CARRIER FOR HIGH FREQUENCY, HIGH POWER CIRCUITS
(Version 1, 150 x 150 mil Cavity, Measurements via HP4191A Impedence Analyzer)

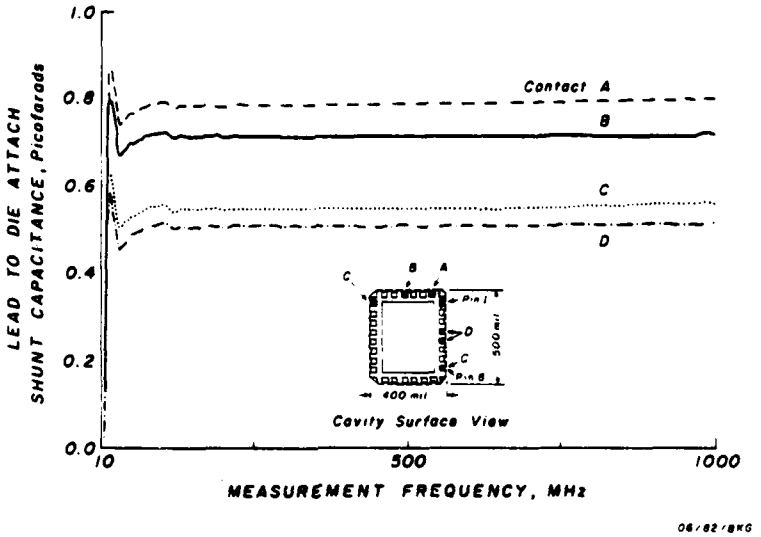


FIGURE 44

ELECTRICAL CHARACTERISTICS OF MAYO-DESIGNED
28-CONTACT LEADLESS CERAMIC CHIP CARRIER
FOR HIGH FREQUENCY, HIGH POWER CIRCUITS
(Version 1, 190 x 250 mil Cavity;
Measurements via HP4191A Impedance Analyzer)

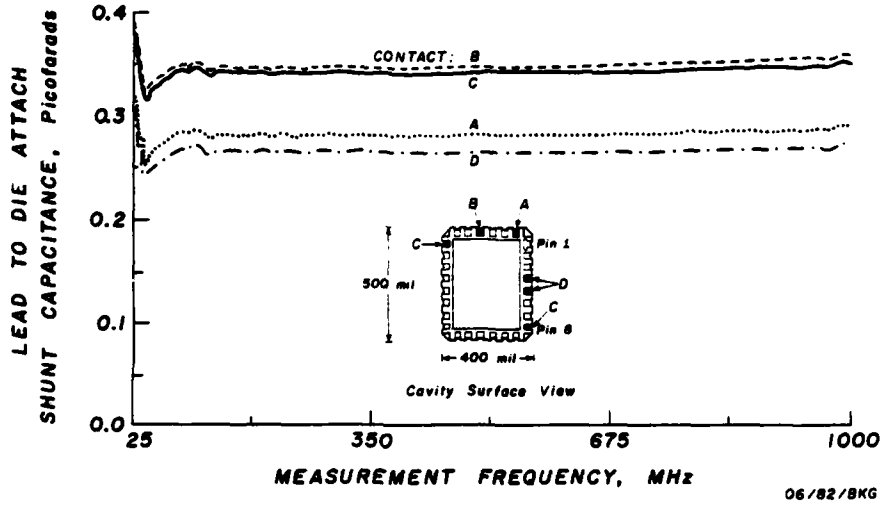


FIGURE 45

Changes To Be Made In Leadless Chip Carrier Design As A Result Of Initial Measurements

A number of modifications are presently in process for the next production run of leadless chip carriers. First, the bonding finger layers of both die-cavity sizes of the leadless chip carrier have been redesigned to achieve the originally

intended effect, i.e., to minimize signal trace width to 10 mils, to maximize intertrace guard band width, and to straighten the traces to minimize average run length, thereby decreasing lead series inductance by about 15%. Several changes in the back layer metallization have also been undertaken. The contact pads on the ceramic back surface of the leadless chip carrier, originally intended to facilitate component testing, add unnecessary shunt capacitance and a short electrical stub to each of the external conductors. These pads will be removed, and only three of the four layers of the castellation will be metallized, thereby further decreasing the stub length.

As noted earlier, the heat spreader design was installed in its particular configuration originally at the request of Fairchild Camera and Instrument Corporation; we have redesigned the back metallization in accord with sound high frequency practice. This change in design will provide lower impedance pathways between the V_{EE} and V_{CC} vias and the locations of the decoupling capacitors on the backs of the chip carriers, and will also provide a more uniform surface area for the lateral distribution of heat through the heat spreader as well as a larger solder attachment point for a copper heat stud. This altered heat spreader design may be observed in the artist's concept of Figures 46 and 47.

The decrease in the dimensional tolerance of the metal contact pads supporting the tungsten bumps, and therefore the possible occurrence of a short circuit during the board soldering

process between the contact pads and the Kovar lid, was considered a serious problem. Since the Kyoto Ceramics engineers were not able to guarantee an improvement in these tolerances, another approach was adopted to minimize the probability of short circuiting. A thicker ceramic layer (layer 4, the tungsten bump layer itself), will be employed in future manufacturing runs, increased from 20 mils to 25 mils. The use of a thicker Layer 4 in turn makes it possible to consider conversion from a 10 mil thick Kovar lid and a metallized seal ring, to a 15 mil thick ceramic lid and a glass frit seal ring. Removal of the metal seal ring will obviate the shunt capacitance from this source. The increase in the thickness in Layer 4 and the conversion to a ceramic lid are related, because the ceramic material is not as strong as the Kovar; a thicker ceramic lid must be used to maintain equivalent strength.

An additional modification will be made in the next production run. Layer one, the die-attach layer, is currently 25 mils in thickness; Mayo had originally specified a thinner die attach layer for better thermal conductivity; Kyoto Ceramics stated initially that their fabrication processes could not guarantee immunity to fracturing for such a thin back surface. Kyoto Ceramics now believes that the die-attach layer thickness can be reduced from 25 mils to 20 mils, and perhaps even to 15 mils; both the 15 mil and 20 mil die-attach layer version will be attempted in the next production run. Conversion from a 25 to a 15 mil thickness for Layer 1 will improve the thermal conductivity of the back surface by 40%.

If the modified chip carriers perform well, we will use them for early studies of the performance of Gallium Arsenide digital integrated circuits. However, as presently manufactured, Gallium Arsenide wafers are usually 25 mils in thickness in comparison to the typical 20 mils used for silicon. All conventional leadless chip carriers employ die-well cavity depths too shallow for use with Gallium Arsenide components. As a result, a portion of the next production run of these leadless chip carriers will be fabricated with a 5 mil deeper die-well cavity.

AIR-COOLED LEADLESS CERAMIC CHIP CARRIER FOR HIGH POWER, HIGH FREQUENCY DIGITAL INTEGRATED CIRCUITS

(28 Pads; Two Die Cavity Versions; Recessed Lid For Mounting Die Well Down; 94% Alumina Substrate)

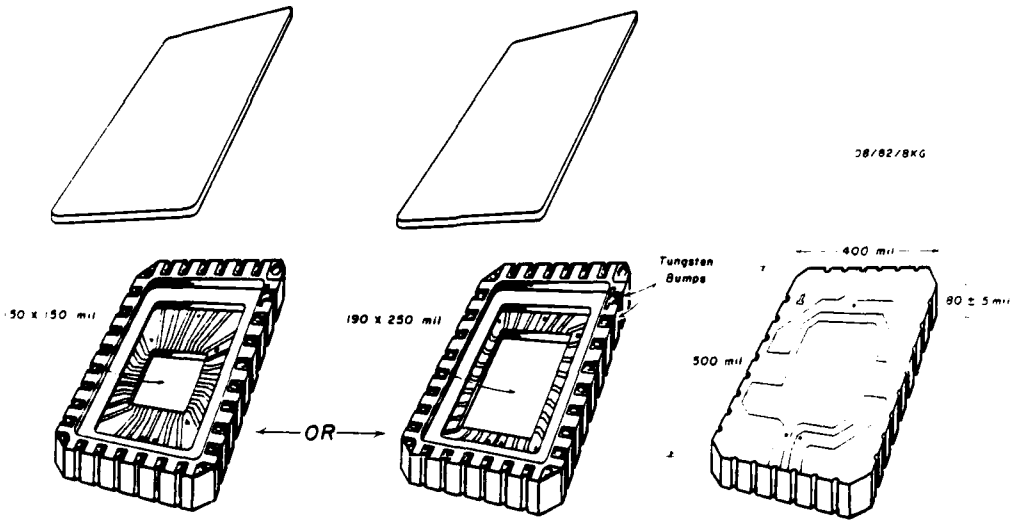


FIGURE 46

AIR-COOLED LEADLESS CERAMIC CHIP CARRIER
FOR HIGH POWER, HIGH FREQUENCY
DIGITAL INTEGRATED CIRCUITS

(28 Pads, Two Die Cavity Versions ;
Recessed Lid for Mounting Die Well Down ;
94% Alumina Substrate)

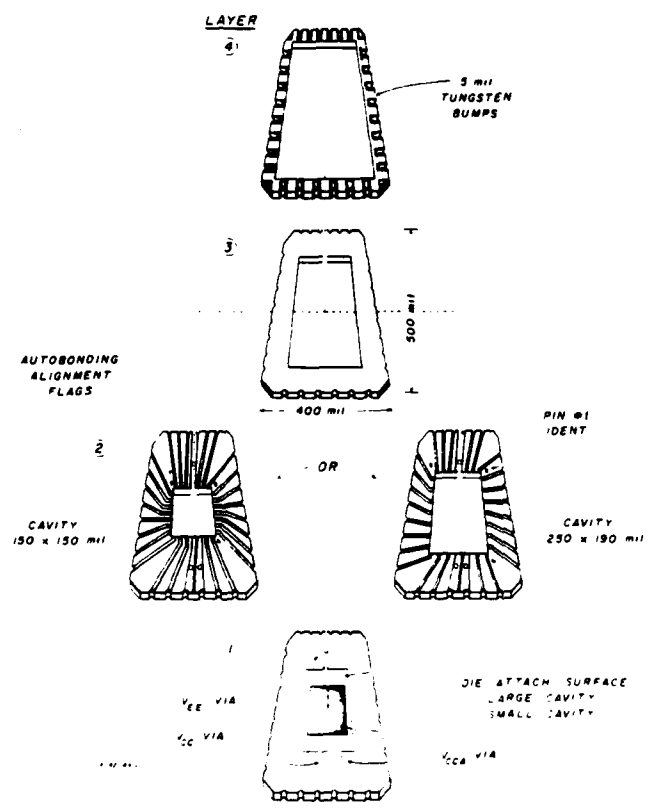


FIGURE 47

In spite of the numerous modifications to be made on the second run of leadless chip carriers, and although the first fabrication run will probably be used primarily for electrical, thermal, and mechanical testing, Fairchild Camera and Instrument Corporation will package approximately 30 integrated circuits in these early version chip carriers, to allow some early performance measurements.

SECTION IV

DESIGN AND DEVELOPMENT OF MULTILAYER WIREWRAP UNIVERSAL LOGIC PANEL OPTIMIZED FOR LEADLESS CERAMIC CHIP CARRIERS

The conversion from the use of 32-pad leadless chip carriers to 28-pad leadless chip carriers required that we redesign the matching logic panel described in the previous yearend report. There was thus the opportunity to rethink the board design based upon new data collected in the late summer and early fall of 1981. The most significant new data appears in Figure 48, in which the frequency-dependent impedance was measured in a variety of small chip capacitors over a frequency range of 1-1,000 MHz. The majority of these high quality chip capacitors show an increase in impedance at frequencies above 50 MHz, with a steadily increasing impedance to between 10 and 40 ohms at frequencies of 1,000 MHz. The small NPO monolithic chip capacitor exhibits the lowest impedance, i.e., 10 ohms, at 1,000 MHz. The series inductance of the metal end cap leads of these chip capacitors dominate at frequencies above 125 MHz; at 1,000 MHz, all but the NPO chip capacitor exhibit impedances which render them useless as decoupling devices. Figure 48 underscores the detrimental effect of series inductance even in structures as small as monolithic chip capacitors. As a result, the logic board designs were modified to accept the installation of high quality chip

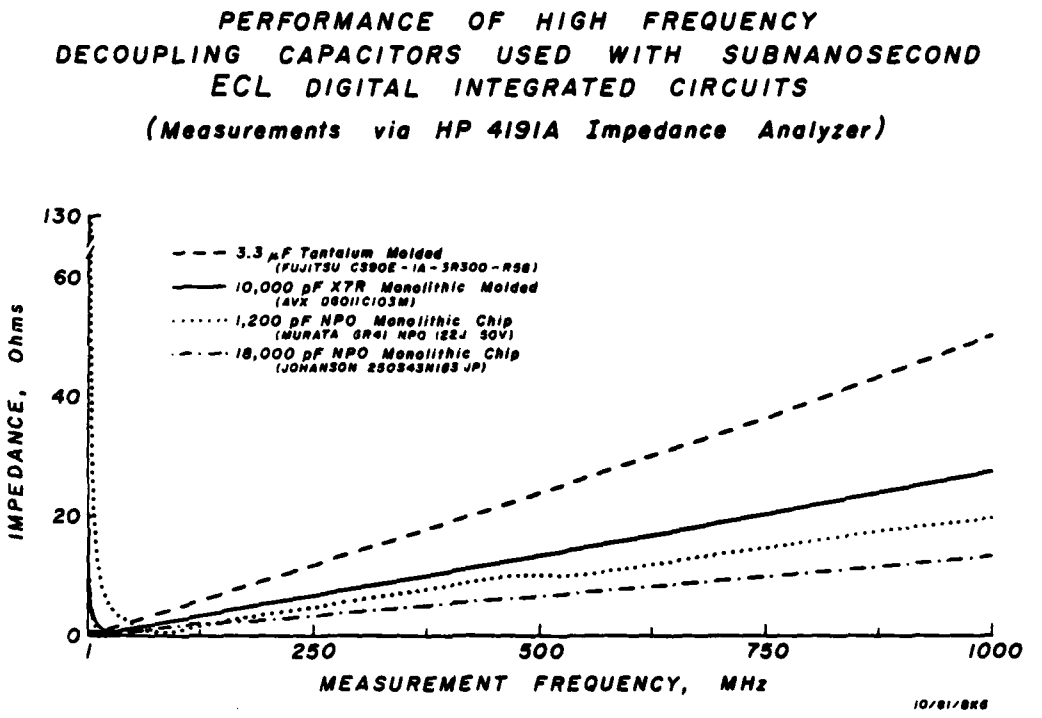


FIGURE 48

decoupling capacitors, rather than the plug-in monolithic capacitors used in our ECL dual in-line package board developed earlier in this project.

Measurements were also performed on the resistor terminator packs developed for the ECL dual inline package circuit board; the series inductances of the metal pins and the long internal common bus of the single inline terminator package (SIP) exhibited extremely poor electrical performance characteristics at

frequencies above approximately 150 MHz. A decision was made to change the design philosophy of the circuit boards, i.e., to abandon the use of specially designed SIP terminator packages, described previously. The component side of the board was redesigned to accept the installation of chip resistors for all terminations.

This new design trades off a gain in electrical performance for a somewhat less convenient installation. As will be described later, supporting data from other studies indicated that the installation of the leadless chip carriers could be performed simultaneously with the installation of terminator chip resistors in a single operation. Furthermore, the computer aided design software used to fabricate these boards will be provided with additional prompting aids that will assist the fabrication technician in the installation of chip resistors at the correct locations on each logic panel. An analysis of several previous designs revealed that on the average, only three chip terminator resistors would have to be installed for each chip carrier installed. This low percentage of required chip resistors made their use attractive in view of their improved electrical performance.

Figure 49 is an artist's conception of a new multilayer wirewrap panel modified for the 28-pad leadless ceramic chip carriers, and adopted to accept discrete high frequency chip resistors and chip capacitors for signal string termination and

HIGH-FREQUENCY MULTILAYER CIRCUIT BOARD SUPPORTING WIRE WRAP INTERCONNECT OF SUBNANOSECOND ECL COMPONENTS ENCAPSULATED IN LEADLESS CERAMIC CHIP CARRIERS

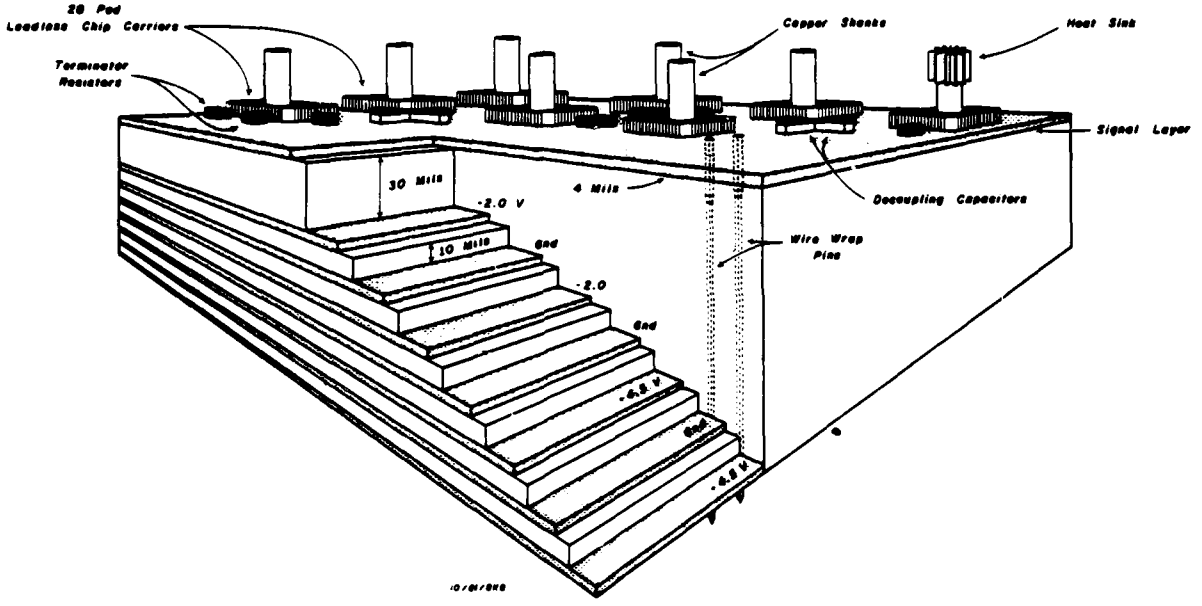


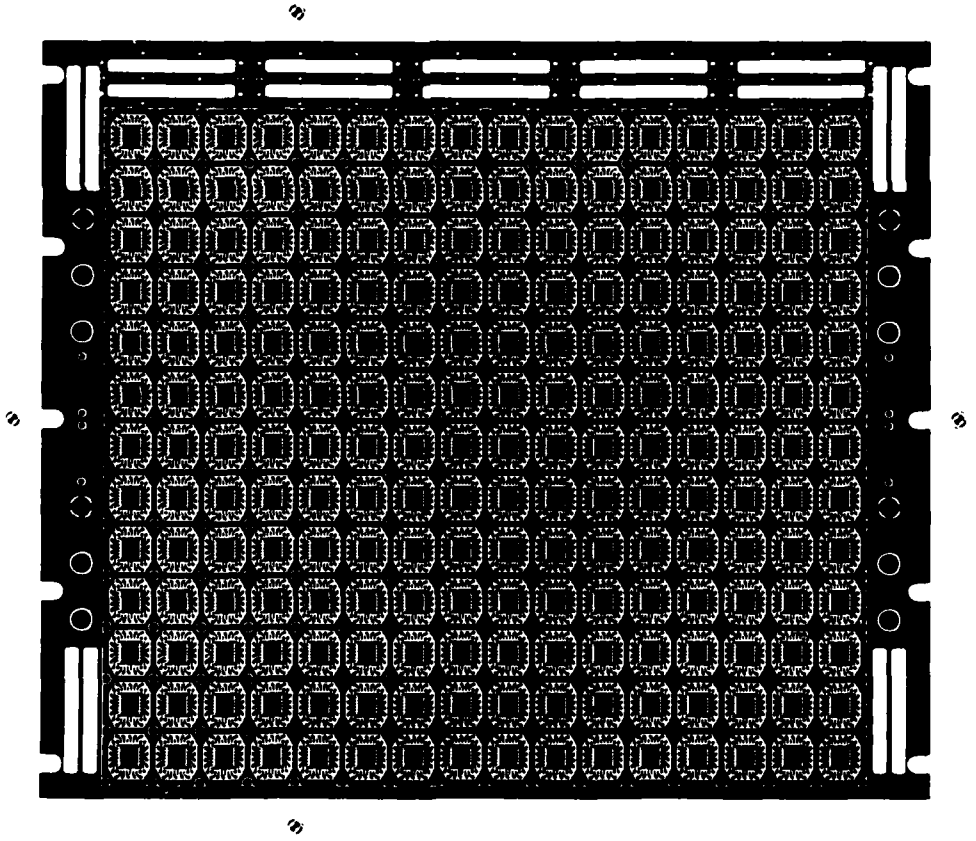
FIGURE 49

decoupling. As in the case of the logic panel described in the previous report, this board is 12" x 14", .122" thick, and consists of eight metal bus layers; 1) the component, or signal, layer; 2) a backplane layer committed to -4.5 volts; and 3) six

buried layers, all of which are dedicated either to GROUND, to -2 volts, or -4.5 volts. The interstices between the metal planes are layers of conventional FR-4 epoxy. The spacing between the component side and the first buried layer, a ground plane, is 30 mils, to create a 75 ohm impedance for the signal traces on the component layer. The spacing layers between the other buried metal planes are each ten mils thick, thereby maximizing the interplane decoupling capacitance while maintaining sufficient thickness of the FR-4 epoxy to minimize pinholes and perforations and the possibility of short circuits between the planes.

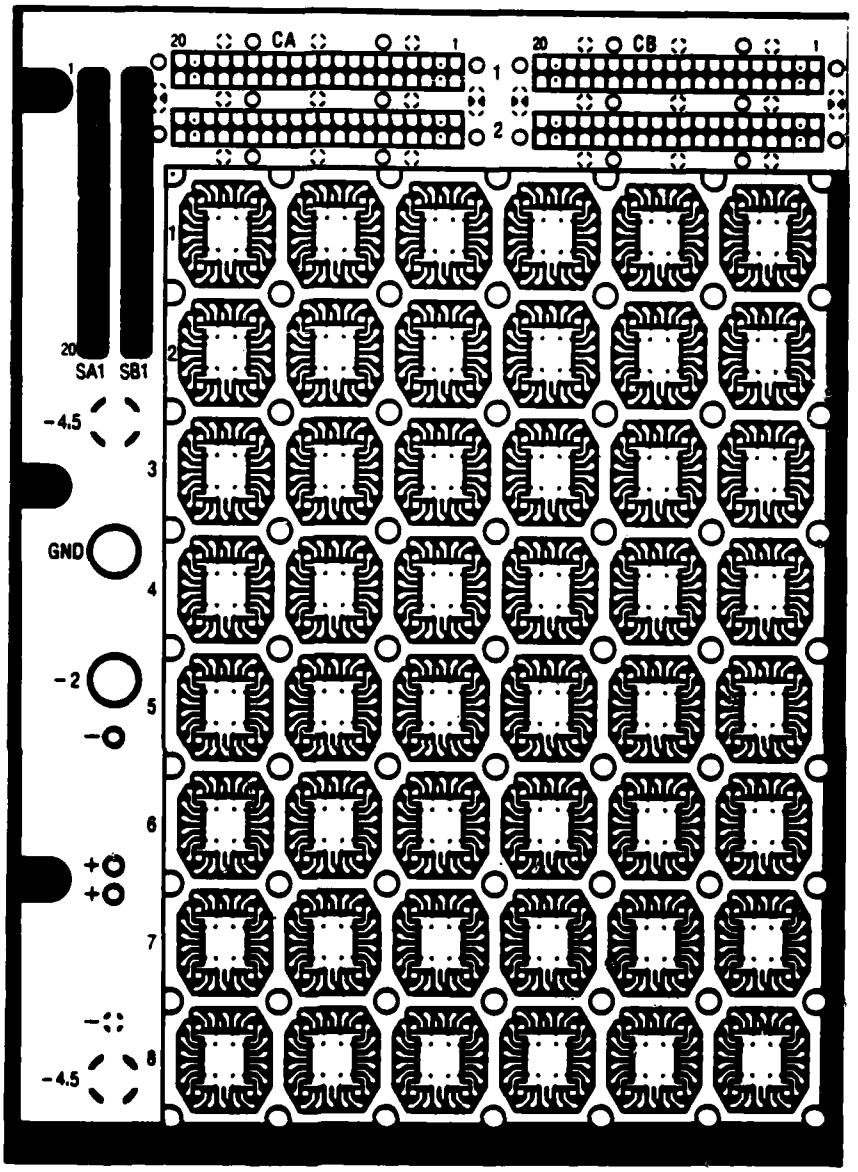
Figure 49 also depicts a small portion of the component layout on the upper surface of the board; the complete array contains patterns to support 208 28-pad LCCCs and associated discrete chip terminator resistors and power plane decoupling capacitors. The component array consists of 16 columns and 13 rows of chip carrier patterns, as well as two horizonal rows of five 40-pin connectors along the upper edge of the board. The left and right edges of the board each contain two sets of power and ground studs; power is thus fed to the board along both of its vertical edges, as depicted in Figure 50, a reproduction of the artwork for the component surface of the board. A more detailed view of the upper left corner of this board is presented in Figure 51. As may be observed in both of these figures, adjacent to the power and ground studs are four sets of DIP sockets which will accept auxiliary components such as 300 mil or 400 mil dual inline packages, DIP switches, or additional connectors.

Figure 52 is an artist's conception of four adjacent chip carrier patterns on the component side of the board, with a 28-pad leadless chip carrier installed in the lower right pattern. Each of the subarrays consists of a leadless chip carrier, surrounded on all sides by headless, flush-mounted wirewrap pins which completely penetrate the board. The heavy metal buses,



PHOTOGRAPH OF PRODUCTION ARTWORK FOR COMPONENT SIDE OF 208-PATTERN LEADLESS CHIP CARRIER BOARD

FIGURE 50



PHOTOGRAPH OF COMPONENT SIDE OF QUARTER SIZE LEADLESS CHIP CARRIER LOGIC BOARD.

FIGURE 51

which surround each pattern in close proximity to the flush mounted heads of the wirewrap pins, are committed during board fabrication to the -2 volt power planes. These foils are the reference buses for the pulldown voltage to which each signal string terminator resistor must be attached. In the lower right panel of Figure 52, seven of these resistors are indicated as

COMPONENT-SURFACE VIEW OF LOGIC PANEL FOR SUBNANOSECOND ECL CIRCUITS PACKAGED IN LEADLESS CHIP CARRIERS

(28-Pad LCCCs; 8-Layer, 12" x 14", 208 Pattern G-10 Board)

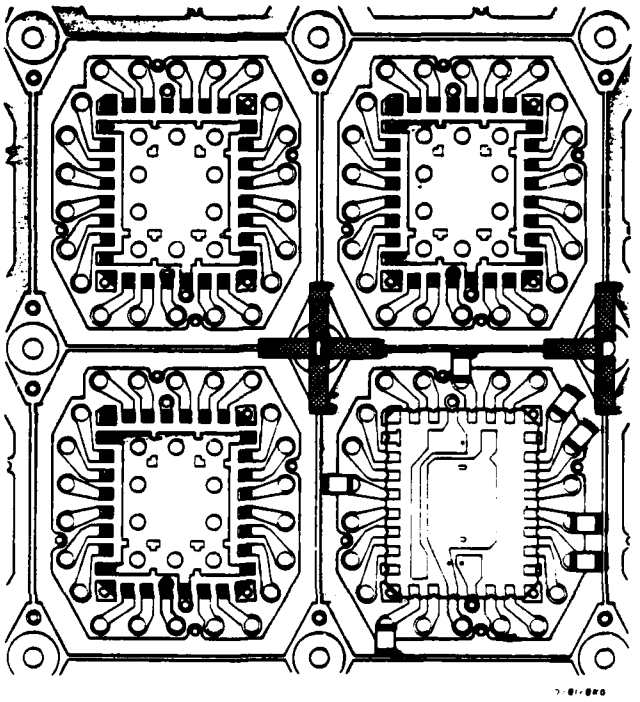


FIGURE 52

white rectangles with black ends. The doughtnut-shaped structures at the corners of each set of four chip carrier patterns are committed at board fabrication time to GROUND; these ground posts are attachment points for four decoupling capacitors for the -2 volt busses. These latter structures are shown as crosshatched rectangles fanning out in a cross shaped pattern in the center of the figure. The three dark rectangular patterns visible in the figure are metallization areas which lie beneath the chip carriers after they have been soldered in place. These metallized areas, which are also connected to GROUND, serve as a partial electromagnetic shield for the chip carrier; in addition, they connect a number of the flush mounted headless pins to one another and to the buried ground planes in the circuit board.

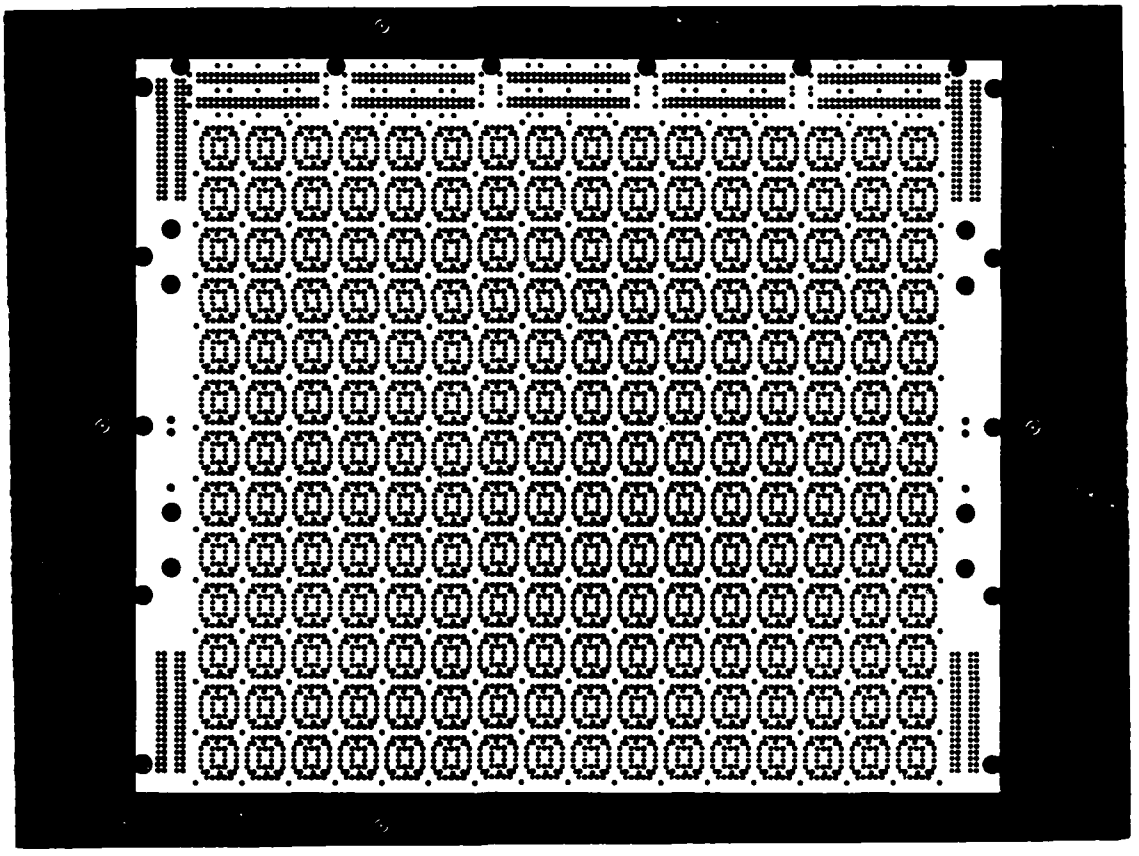
As alluded too earlier, a foil trace approximately 200 mils in length on the printed circuit board conducts a signal from each tungsten solder bump on the bottom of the leadless chip carrier to a circular island. Each island is the head of a flush mounted wirewrap pin which penetrates the board without making contact with any of the buried layers. These wirewrap pins are headless, machined brass, square cross section pins plated with a gold-over-nickel layer; no two pins are closer than 100 mils to one another. On the component side of the board, the foil trace passes over the top of the flush mounted head of the wirewrap pin. If a termination is needed for a given signal pin, a chip resistor is placed between the end of the signal trace and the -2 volt bus foil which surrounds the pattern. Ground and -4.5 volt

bus connections are supplied to each leadless chip carrier by means of solid plated-through holes penetrating to the appropriate power and ground layers of the board.

The array patterns on the component side of the circuit board permit direct solder bonding of the leadless chip carriers, discrete chip terminator resistors, and chip decoupling capacitors to the panel; if necessary, conventional 24-pin leaded flat packs can also be installed in any subarray pattern in place of a leadless chip carrier. Considerable effort has also been expended to assure that this logic board will except the installation of special components which require signal, power, or ground attachments in "nonstandard" locations with an absolute minimum of special board preparation. Every one of the 28 padouts to each leadless chip carrier, as well as the four corner padouts, may be used as a signal, a power contact (either -2 volts or -4.5 volts, as required), or a ground contact.

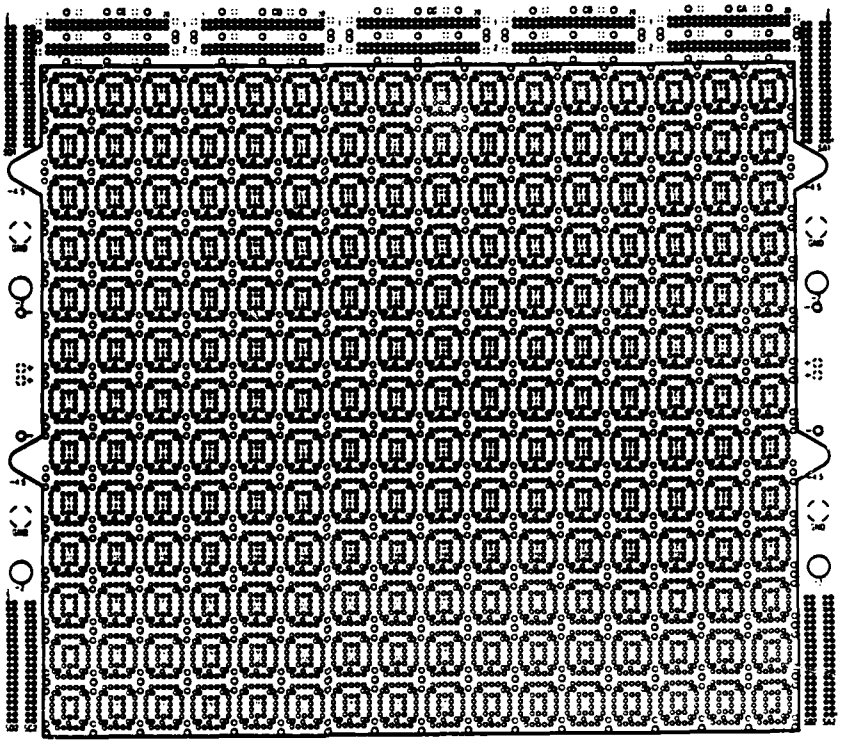
Figures 53 through 61 depict the artwork for the full scale 208 pattern board, as well as nine-pattern exploded views of these layers, respectively, for the buried -2 volt, -4.5 volt, and the bottom surface -4.5 volt planes. The goal of this new board design was the achievement of a total foil area for each bus which, computed on a "per-dice" basis, would be no less than that employed in the dual inline package (DIP) board described in a prior yearend report. Since the average density of ECL dice per unit area on the new leadless chip carrier board will be

higher than for the DIP board, calculations indicated that two or more metal layers in the board would have to be committed to each of the power buses, and connected to one another at numerous locations by solid vias. As was reported in Table 2, Page 90 of the Year Two Interim Report, calculations based upon the chip carrier footprint and layout of the voltage planes, including the effects of the vias on each bus, demonstrated that seven bus layers and a signal layer would be required, with an alternation of layers as depicted in the artist's conception, Figure 49.



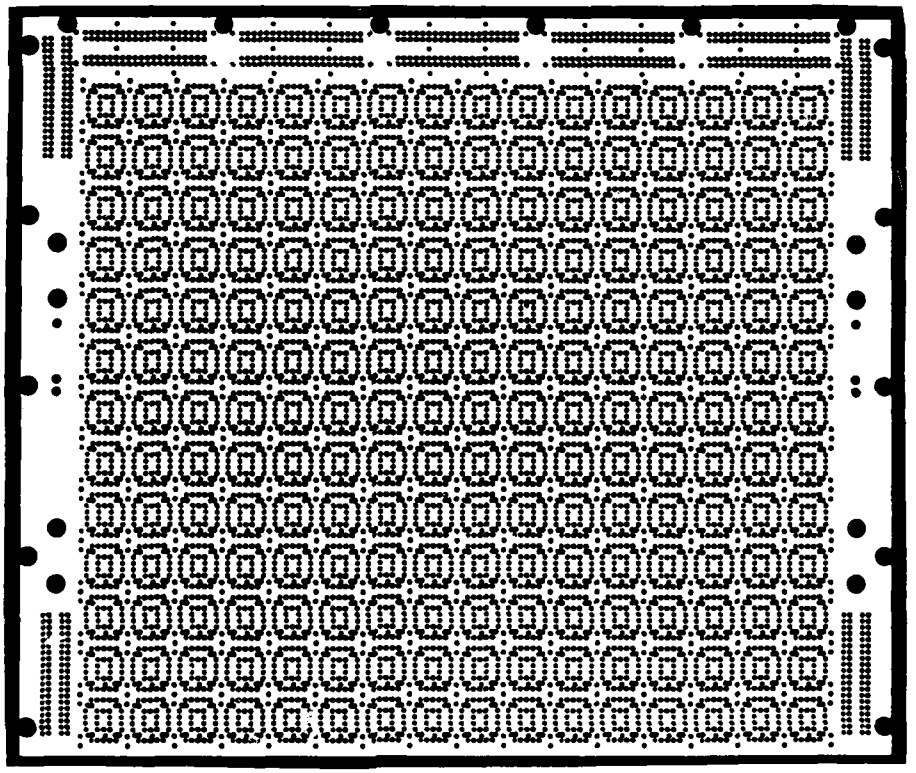
ARTWORK FOR -2 VOLT BURIED LAYER POWER PLANE FOR 208-PATTERN LCCC LOGIC BOARD.

FIGURE 53



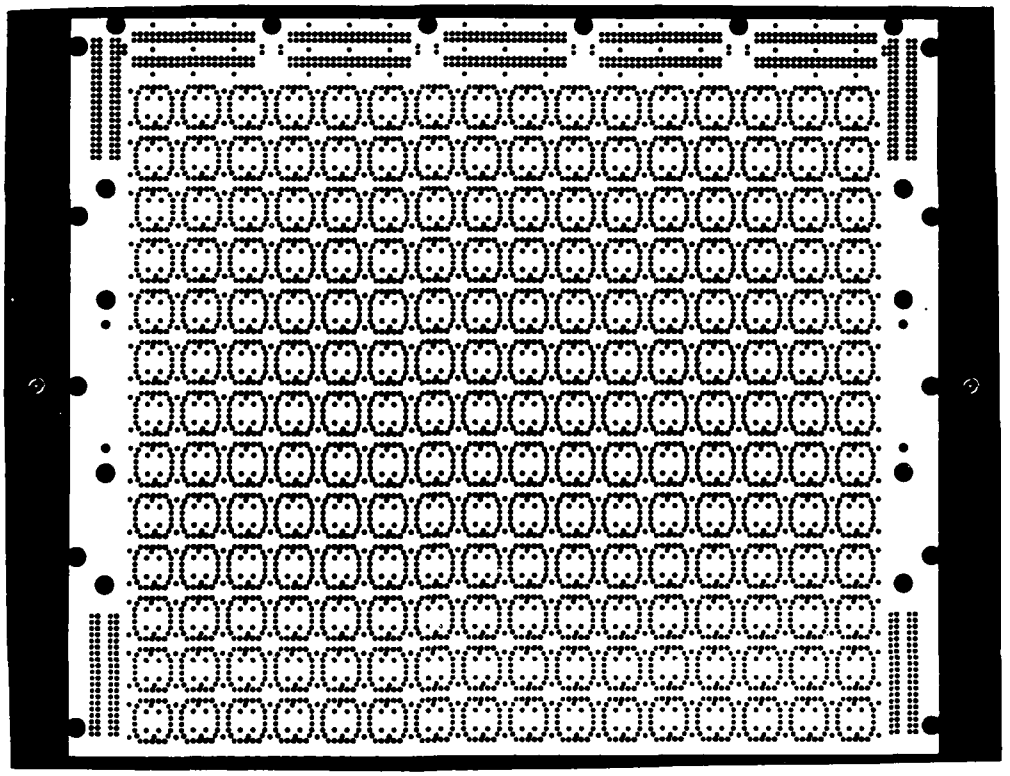
ARTWORK FOR -4.5 VOLT BOTTOM-SURFACE (WIRE-WRAP SIDE) POWER PLANE FOR 208-PATTERN LCCC LOGIC BOARD.

FIGURE 54



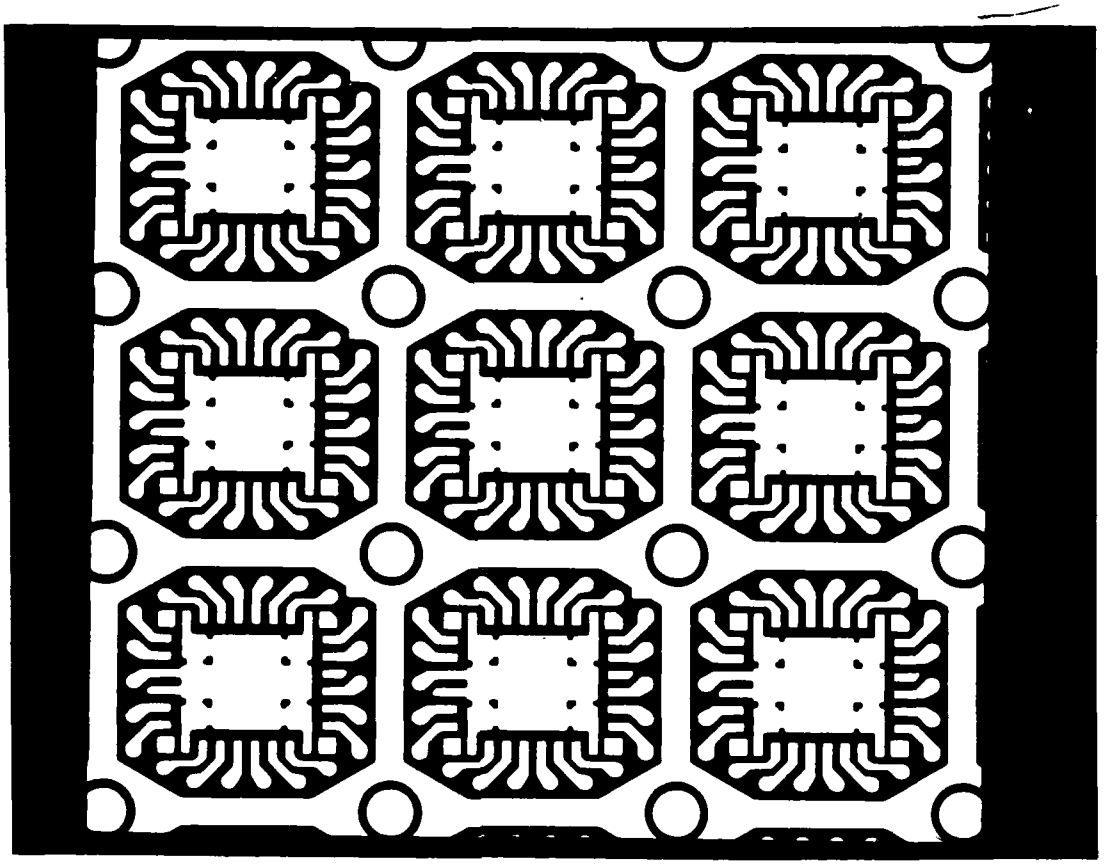
ARTWORK FOR -4.5 VOLT BURIED LAYER POWER PLANE FOR 208-PATTERN LCCC LOGIC BOARD.

FIGURE 55



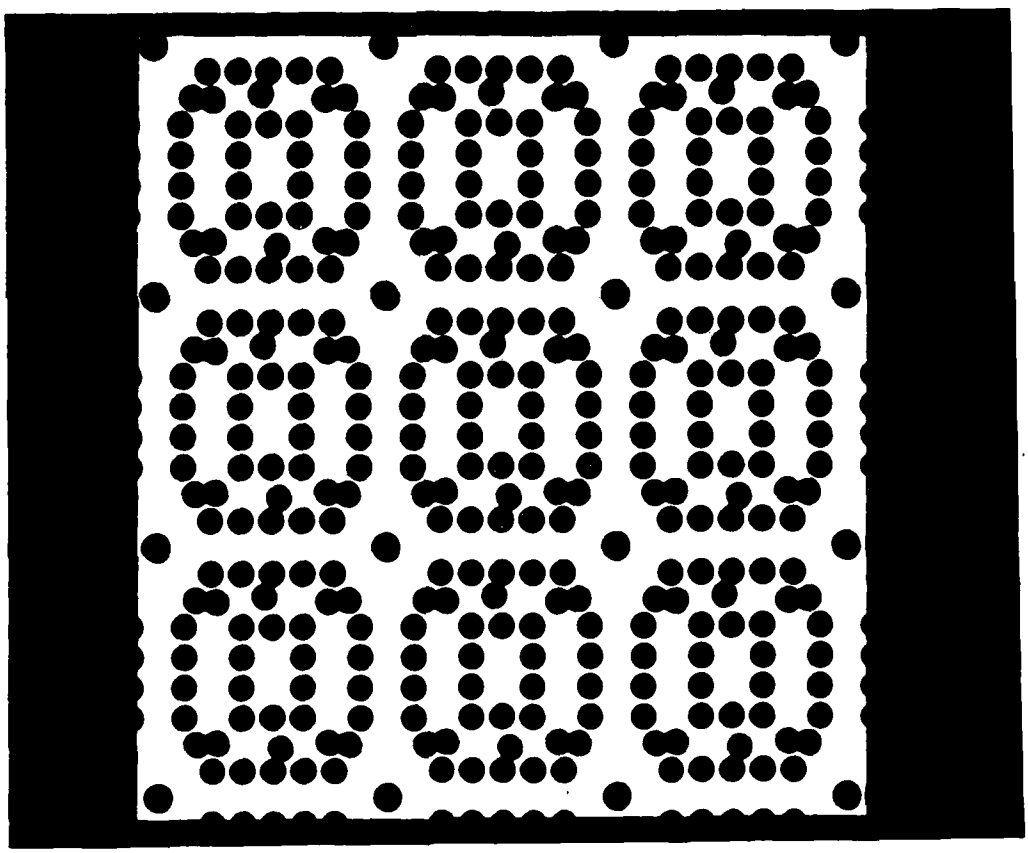
ARTWORK FOR BURIED LAYER GROUND PLANE FOR 208-PATTERN LCCC LOGIC BOARD.

FIGURE 56



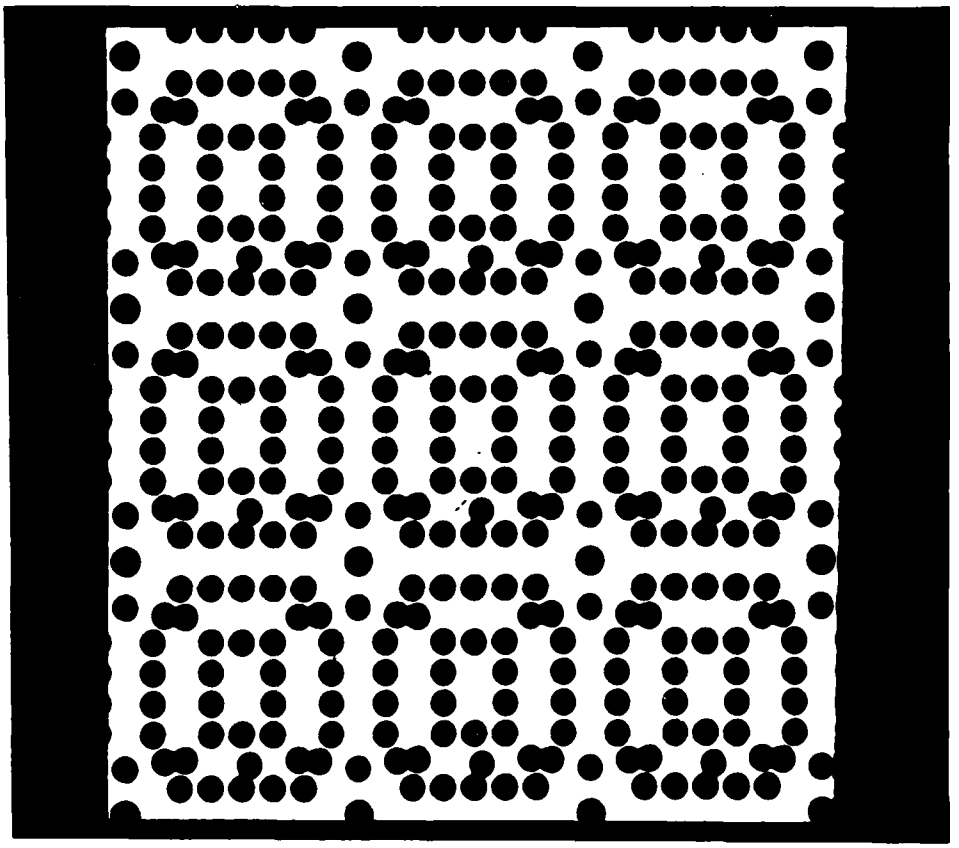
MAGNIFIED VIEW OF COMPONENT SIDE OF LCCC LOGIC BOARD.

FIGURE 57



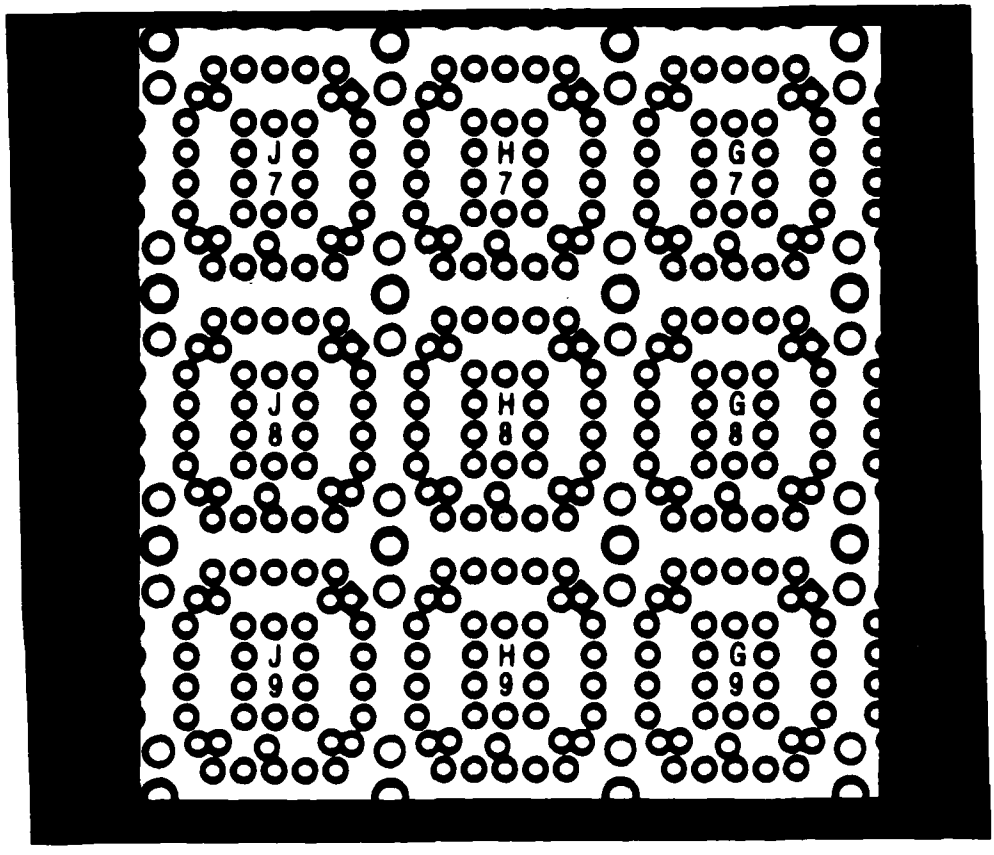
MAGNIFIED VIEW OF -2 VOLT BURIED LAYER POWER PLANE FOR 208-PATTERN LCCC LOGIC BOARD.

FIGURE 58



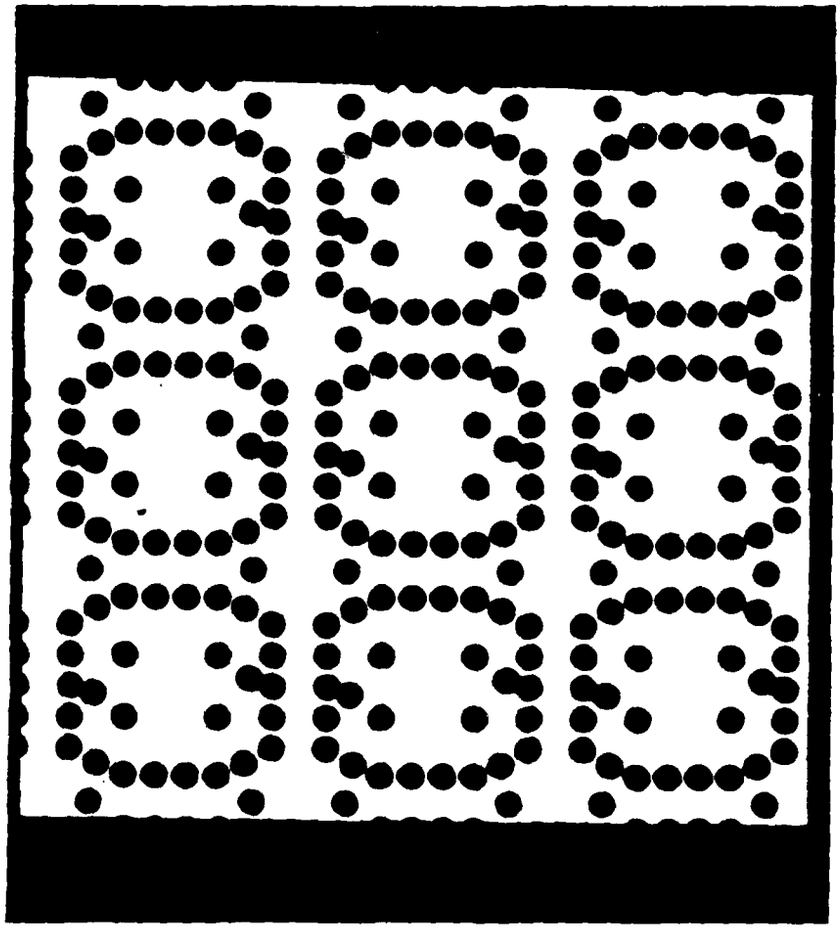
MAGNIFIED VIEW OF -4.5 VOLT BURIED-LAYER POWER PLANE FOR 208-PATTERN LCCC LOGIC BOARD.

FIGURE 59



MAGNIFIED VIEW OF -4.5 VOLT BOTTOM SURFACE (WIRE-WRAP SIDE) POWER PLANE FOR 208-PATTERN LCCC LOGIC BOARD.

FIGURE 60



MAGNIFIED VIEW OF BURIED LAYER GROUND PLANE FOR 208-PATTERN LCCC LOGIC BOARD.

FIGURE 61

TABLE 3

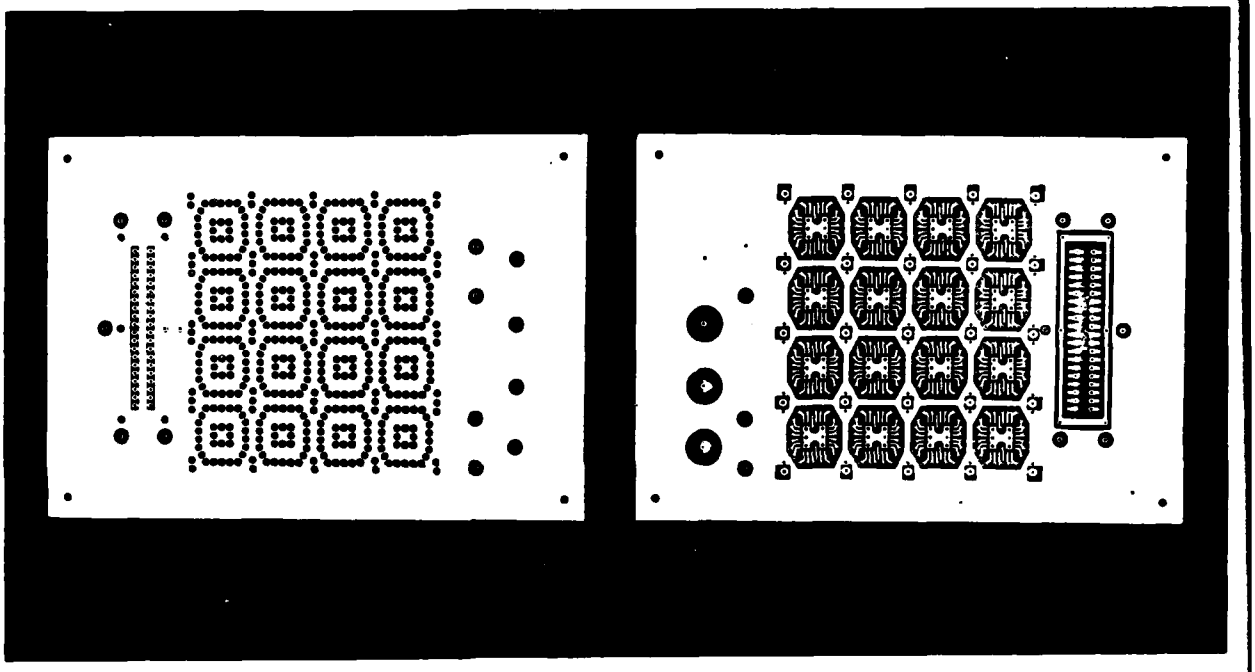
POWER PLANE AND GROUND FOIL AREA COMPARISONS BETWEEN THREE-LAYER DIP BOARD AND EIGHT-LAYER LEADLESS CHIP CARRIER BOARD FOR SUBNANOSECOND ECL COMPONENTS IN 28-PAD LEADLESS CHIP CARRIERS (LCC)

[ALL VALUES NORMALIZED TO PER-CHIP AREAS]

	Ground Bus	-2 Volt Bus	-4.5 Volt Bus
DIP Board Total Foil Area, In^2	.640	.78	.77
LCC Board Total Foil Area, In^2	1.491	.934	.930
LCC Board Percent Improvement	132	19	20
DIP Board X-Dimension Foil, In	.278	.460	.460
LCC Board X-Dimension Foil, In	.780	.580	.520
LCC Board Percent Improvement	180	26	13
DIP Board Y-Dimension In^2	.355	.380	.381
LCC Board Y-Dimension In^2	.960	.700	.740
LCC Board Percent Improvement	170	84	94

The calculations for the redesigned 28-contact leadless chip carrier board are presented in Table 3. These calculations take into account the total area of each layer, and the average path width in both the X and Y coordinates of the board. Since no single metric adequately characterizes the foil area, and thus the electrical behavior of the board, all three metrics were employed to select the number of power planes incorporated into the board design. The reasons for these precautions were outlined in both the Year One and Year Two Interim Reports, on pages 69-71 and 88-89 respectively. Briefly, the impedance of the return current paths must be minimized wherever possible, particularly at the high signal high frequencies expected to be present in these boards, in which even small inductances of 2 or 3 nH can cause large instantaneous voltage drops to appear between two locations on any given power or ground plane. With the higher packing density of the leadless chip carrier board in comparison to the DIP board, higher return path current densities per unit area must be accommodated.

Figure 51 is a view of the upper left corner of the entire circuit board (and incidently, a 48-pattern version of the larger board, which will be manufactured first), in which one additional feature may be identified. The left and top outer margins of the circuit board have a metal foil which is separated from the chip carrier array, as indicated by the horizontal and vertical dark lines which represent guard bands etched through the foil. During the analysis of the new board, it became apparent that an increase



WIRE-WRAP SIDE AND COMPONENT SIDE VIEW OF SMALL BRASSBOARD USED TO TEST ALTERNATE DIFFERENTIAL SIGNAL TRANSMISSION PROTOCOLS.

FIGURE 62

in component density could be achieved if the constraint to provide -4.5 volt busses around every chip carrier could be removed. The -4.5 volt supply is used when a differential signal must be transmitted off-board; one end of both members of a pair of 470

ohm chip resistors must be returned to -4.5 volts to serve as references for the true and complement sides of the differential signal.

It was ascertained that the installation of 470 ohm resistors at the site of the cable connector, rather than at the true and complement output pins of the integrated circuits, will work well provided that the distance between the outputs on the integrated circuit and the connectors is not more than three inches. The round trip propagation delay between the output pins and the pulldown resistors will be less than 700 psec, and will not degrade the offboard wavefronts. This assumption was verified by establishing leadless chip carriers on the small brassboard depicted in Figure 62 and performing wavefront measurements with the pulldown resistors at both locations. To permit the installation of pulldown resistors at the connector, the component-side foils on the outer margins of the circuit board are committed to -4.5 volts through vias penetrating to the -4.5 volt layers. Another advantage of this approach is that if a larger number of 40-pin connectors are required than available on the standard board, a supplementary connector strip can be manufactured with top and bottom foils; these foils can then be electrically connected to the top and bottom surface -4.5 volt foils on the board edge.

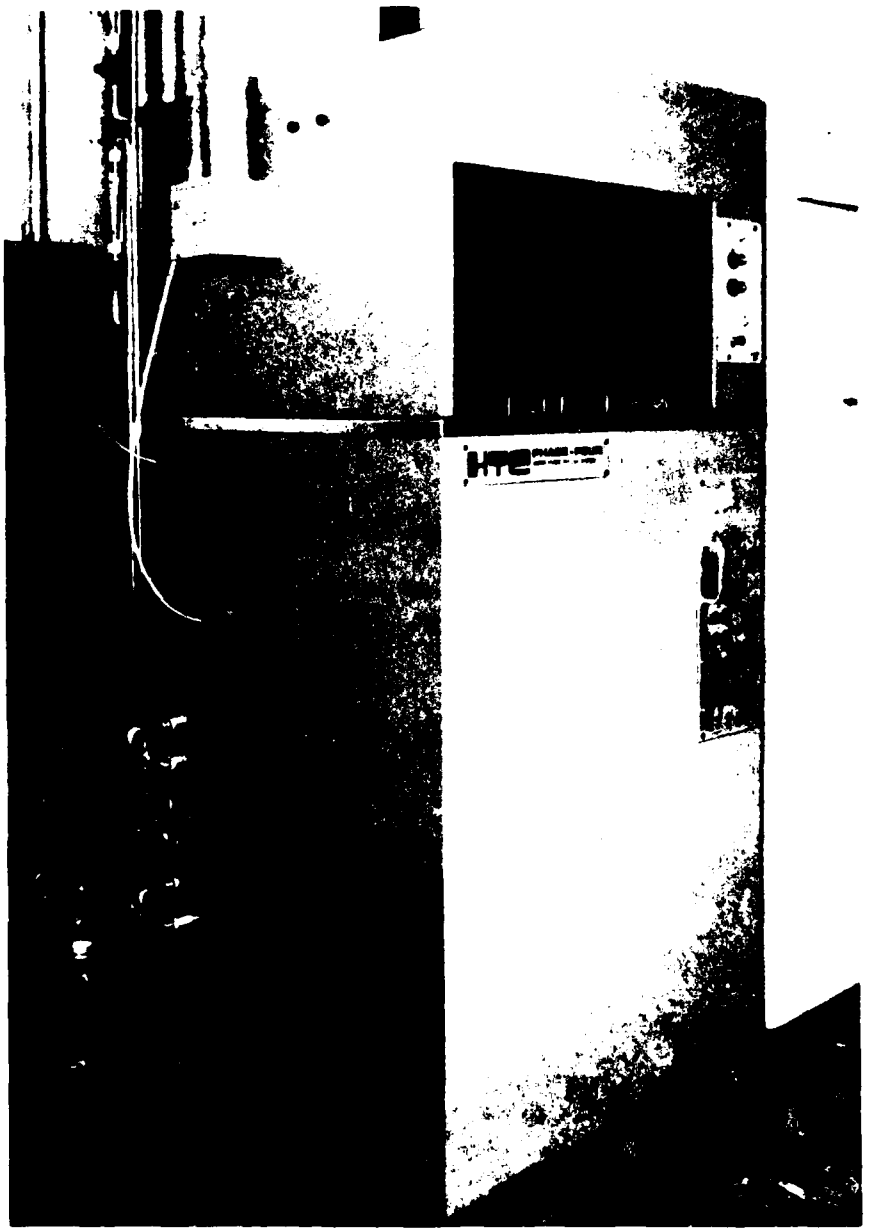
The board design described above was released to Augat, Inc., in January 1982, for a fabrication bid. Augat "no-bid" the design, citing the high cost of initial tooling. The design has been released to an alternate fabricator, Systek, Inc. This vendor has prepared the artwork for the board and is fabricating our

first small production run. To verify correct electrical performance of the design while minimizing costs, the first boards will be 48-pattern subsections of the full-size 208 pattern leadless chip carrier board. The artwork need not be modified for the large boards; it should be possible to identify on the small boards generic problems which can be corrected before the large production boards are fabricated. This first batch of five 48 pattern boards should be delivered by the end of August, 1982.

SECTION V

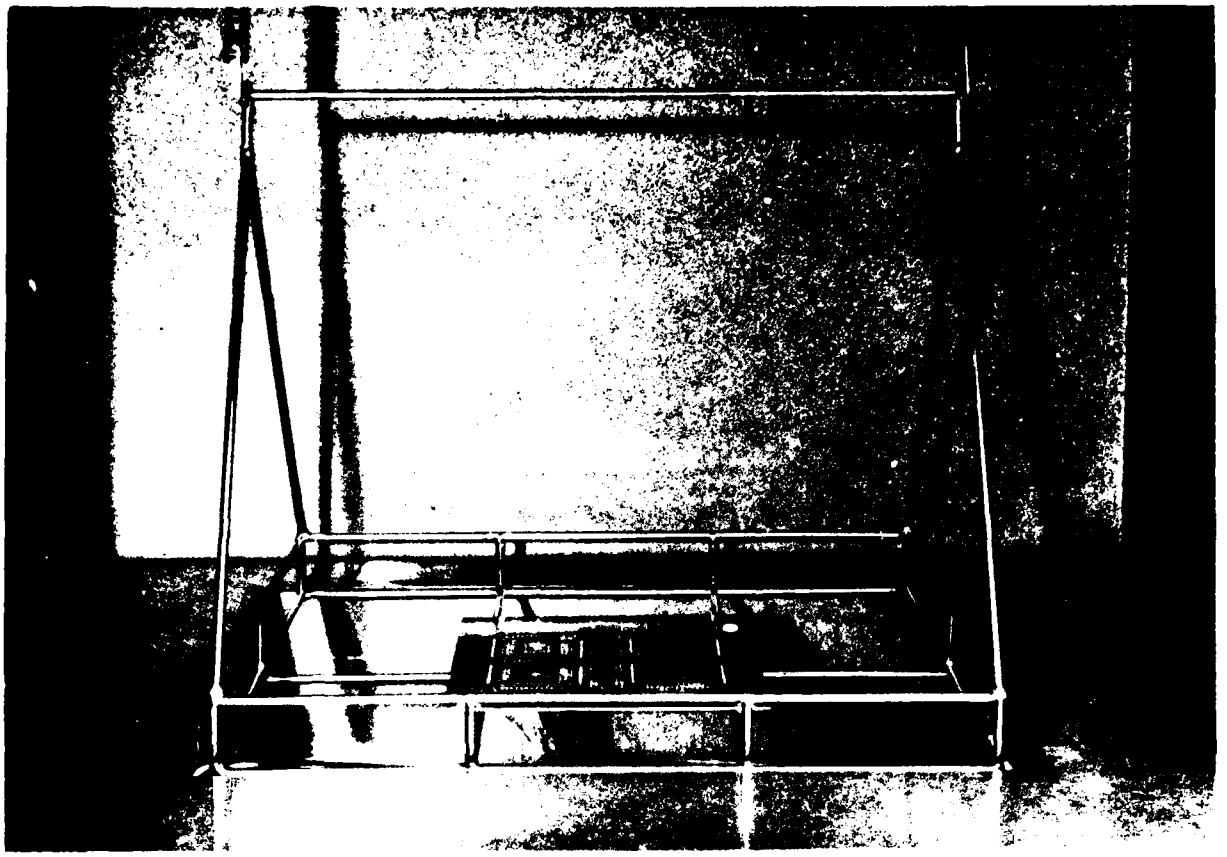
TECHNIQUES OF BONDING LEADLESS CERAMIC CHIP CARRIERS TO MULTILAYER CIRCUIT BOARDS

In August, 1981, a Hybrid Technology Corporation Model 1214 Vapor Phase Reflow Machine was acquired by this laboratory (Figures 63 and 64). A series of tests was undertaken to determine the best way to attach different types of components to printed circuit boards. Figure 65 shows the results of soldering nine small leadless ceramic chip carriers, and a number of miniature chip resistors and chip capacitors, to a circuit board in a single operation. These chip carriers were specially fabricated for this test with 5 mil tungsten bumps on their undersides. The nine chip carriers contained a total of 216 contacts; following the soldering operation, not a single short circuit or open circuit was detected. Likewise, all chip resistors and chip capacitors were soldered correctly on the first pass. Different solder formulations were employed in this test; the results were similar to those reported in the Year Two Interim Report regarding the wetting characteristics of the various solder materials. Figure 66, a photomicrograph of the center chip carrier in the pattern of nine, shows the good wetting and low level of solder bleeding around each of the chip resistors and chip capacitors. Figure 67 is an expanded photomicrograph of the same chip



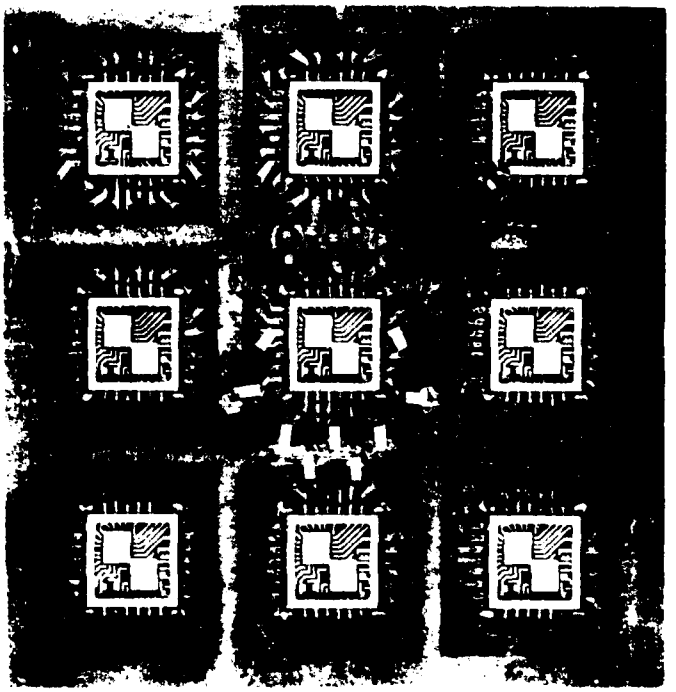
HYBRID TECHNOLOGY CORPORATION MODEL 1214 VAPOR PHASE REFLOW SOLDER MACHINE. THIS DEVICE CAN SOLDER ALL COMPONENTS ON BOARDS AS LARGE AS 12" x 14" IN A SINGLE 30-SECOND OPERATION.

FIGURE 63



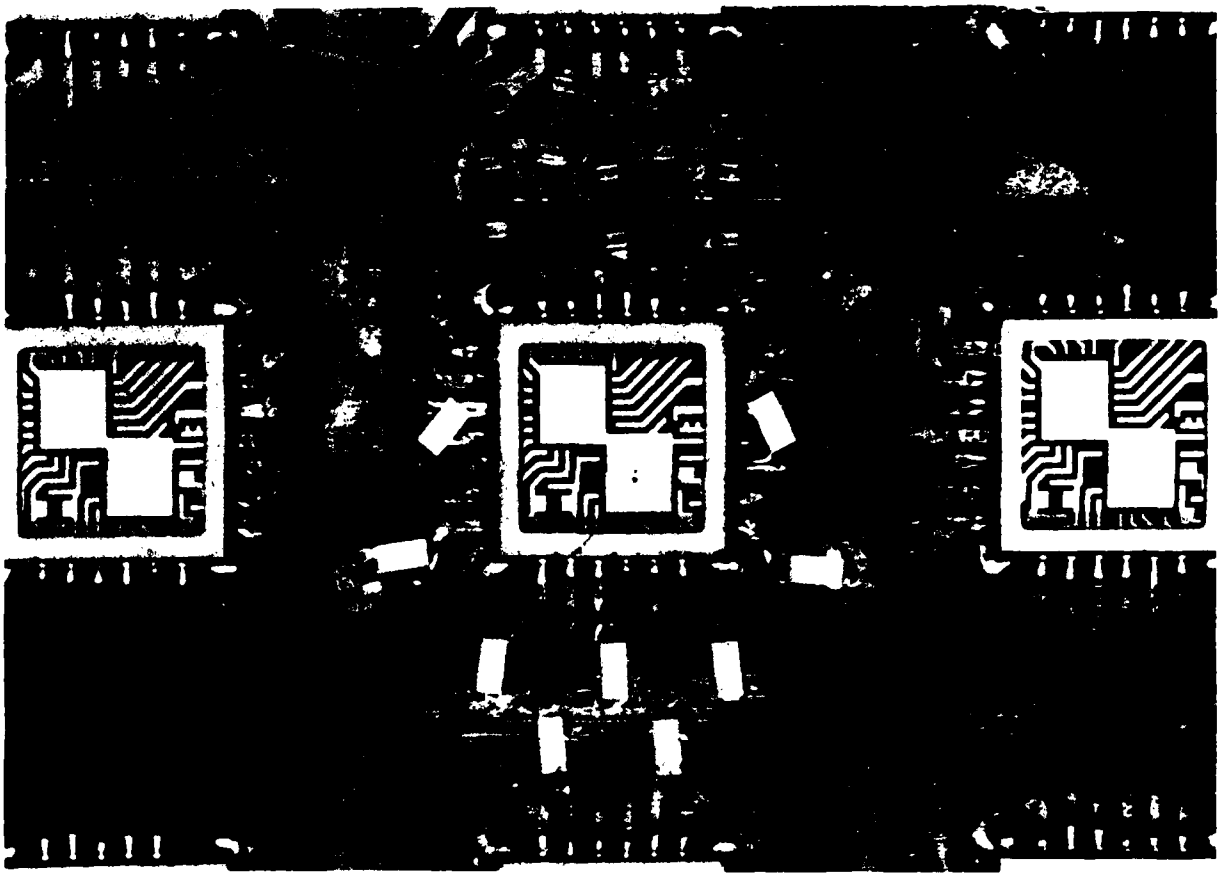
CLOSEUP VIEW OF THE SUPPORT BASKET AND CHAIN PULLEY OF HYBRID TECHNOLOGY CORPORATION MODEL 1214 VAPOR PHASE REFLOW SOLDER MACHINE. NOTE SMALL LOGIC BOARD IN BASKET.

FIGURE 64



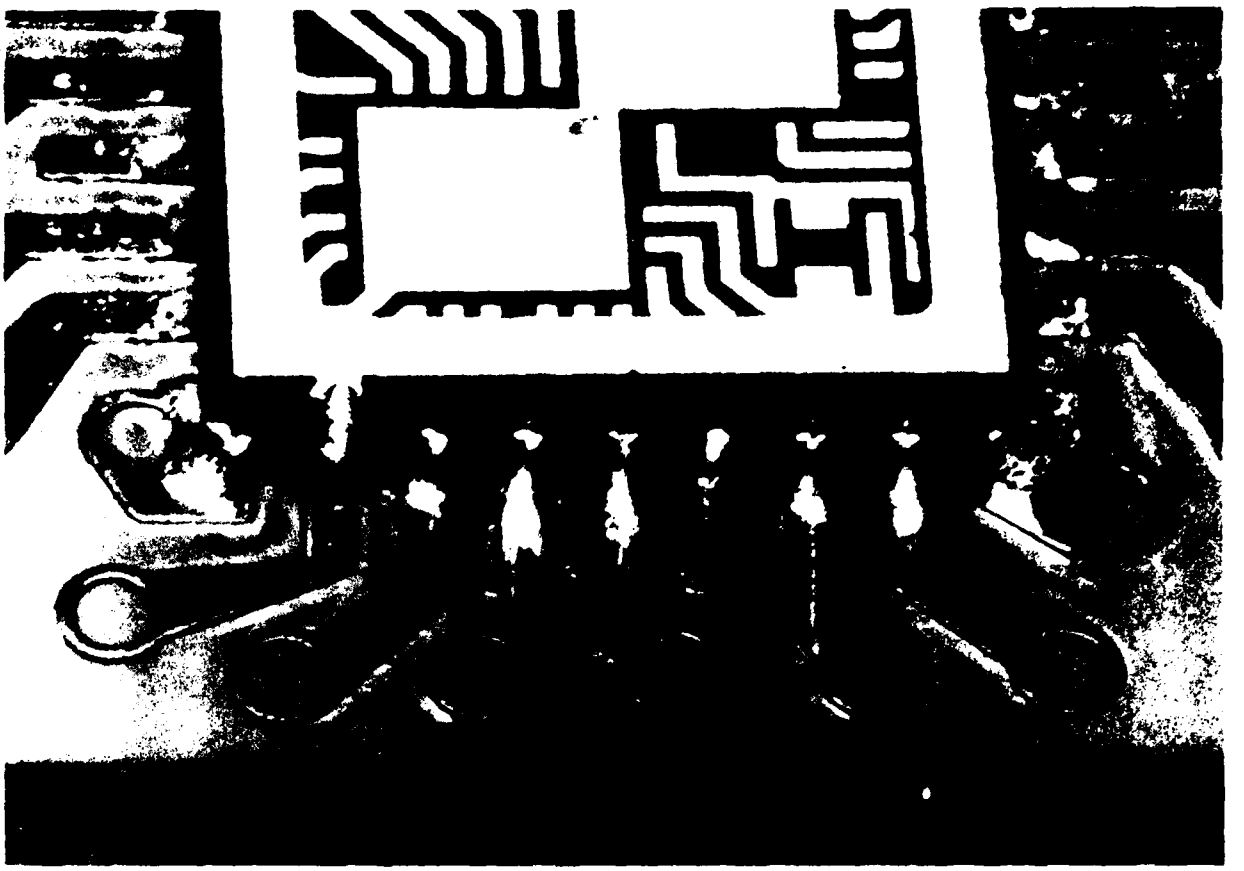
CIRCUIT BOARD USED TO VERIFY SIMULTANEOUS SINGLE PASS VAPOR PHASE REFLOW SOLDERING OF TYPICAL COMPONENTS.

FIGURE 65



EXPANDED PHOTOGRAPH OF CENTER PATTERN OF CIRCUIT BOARD USED FOR VAPOR PHASE REFLOW SOLDER TESTS.

FIGURE 66

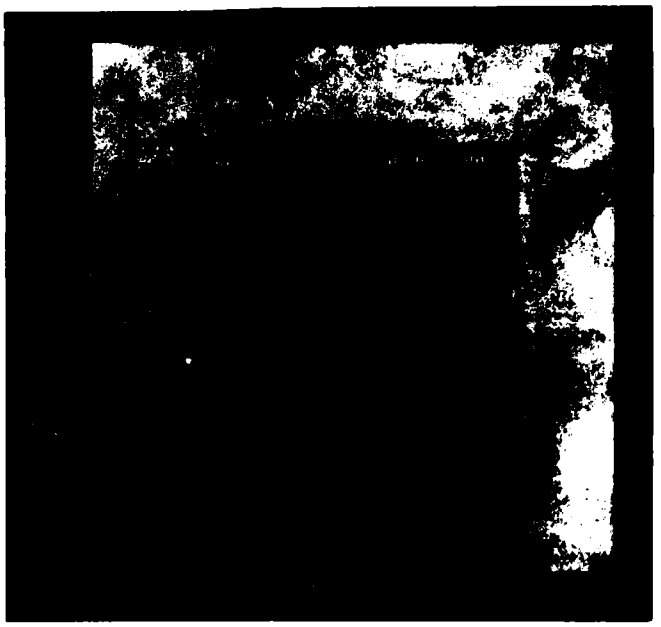


PHOTOMICROGRAPH OF SOLDER FILLET JOINTS BETWEEN TEST CIRCUIT BOARD AND TUNGSTEN-BUMPED LCCCs. AN EXCESSIVE AMOUNT OF SOLDER CREAM WAS APPLIED.

FIGURE 67

carrier shown in Figure 66; note that that no solder bridges or whiskers have formed between any of the contacts. The results of this test indicated that a smaller quantity of solder cream should have been applied to each contact

Because of the increasing use of VLSI components, it is becoming necessary to employ large leadless chip carriers with 120-220 separate contacts. However, a prohibitively large leadless chip carrier would result if a considerable number of



SOLDER TEST BOARD FOR EXPERIMENTAL 180-PAD LEADLESS CERAMIC CHIP CARRIER. PLATED-THROUGH HOLES AND SOLID VIAS ALLOW INTEGRITY TESTING OF SOLDER BONDS ON INNER ROWS.

FIGURE 68

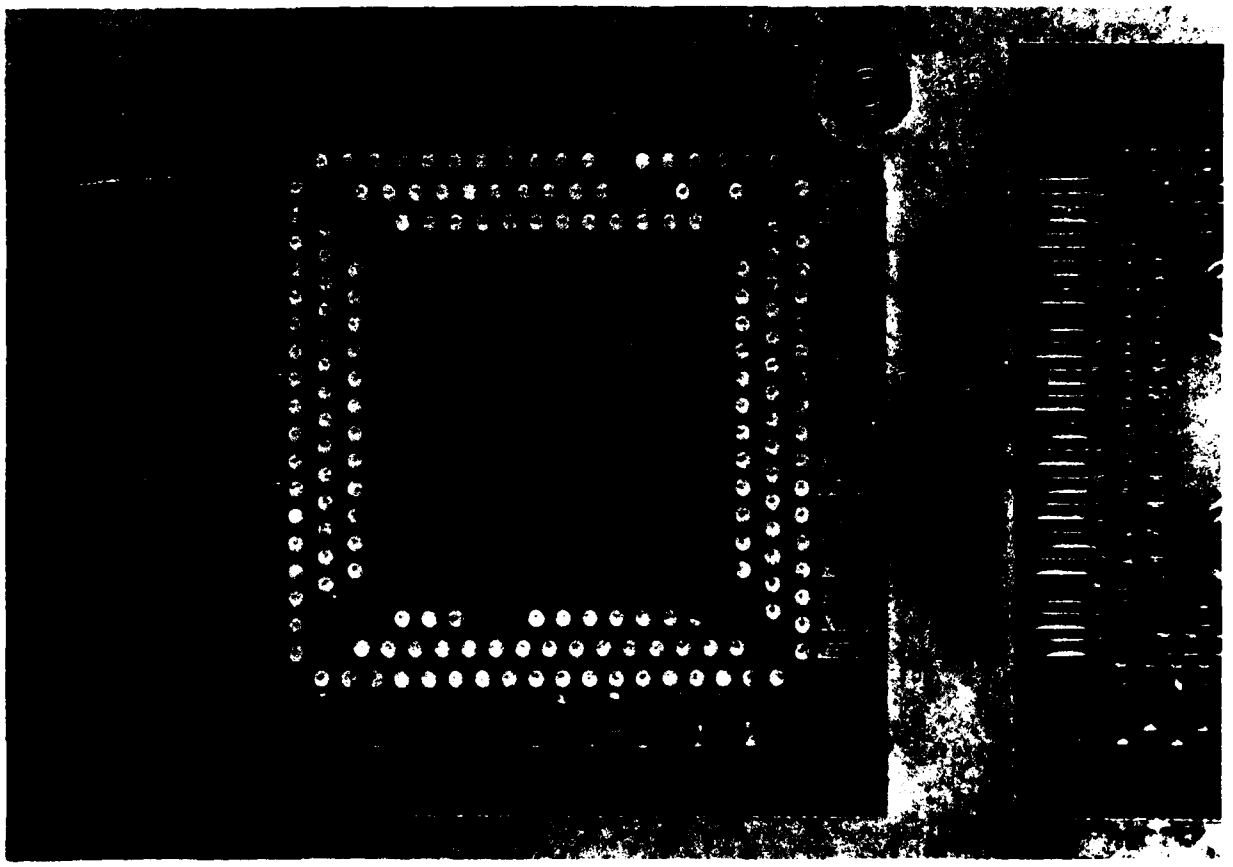
contacts were to be placed along the edges of the carrier in a single row. We have therefore considered the possibility of placing contacts on the under surface of the leadless chip carrier in two or even three concentric rows. However, there is then no guarantee that even Vapor Phase Reflow solder techniques will assure correct attachment of all elements in the inner rows of contacts. At the least, inspection of these blind solder attachments can be made feasible by allowing the contacts to

penetrate to the upper surface of the leadless chip carrier by means of a solid via; DC testing can then reveal if one or more of the solder joints is incomplete; short circuits between adjacent pads should also be detectable.

In order to test this possibility, a special ceramic test blank was fabricated containing 180 contacts in three rows, with the contacts penetrating the body of the test blank. A matching circuit board was also fabricated with solder pads and via holes penetrating the board, allowing direct continuity testing to be performed for each contact between the bottom of the board and the contacts on the upper surface of the test blank. Figure 68 shows this small test board with one of the test blanks prior to the soldering process. Figure 69 is a close-up view of one of these test blanks soldered in place on the circuit board. Of the 180 solid vias, only seven pads did not solder correctly (these pads were marked with ink); all failed joints were open circuits, with no short circuits between adjacent pads detected.

Through an error in manufacturing, tungsten bumps were not electroplated onto the backs of these test blanks. These test blanks are now being modified and remanufactured with 5 mil tungsten bumps on each of the contact pads; the solder test will be repeated with the improved structures. Nonetheless, these early results are quite encouraging, since only a small amount of solder cream was applied to each of the contact pads, and no

great care was taken to assure accurate placement of each small aliquot of paste. If further testing reveals that this approach to the bonding of high density components to a circuit board is viable, the results can form the basis of the design of a new series of a high pad count leadless chip carriers.



PHOTOMICROGRAPH OF RESULTS OF VAPOR PHASE REFLOW SOLDERING OF TEST BLANK WITH THREE ROWS OF CONTACTS. INKED CONTACTS (7 TOTAL) FAILED TO REFLOW.

FIGURE 69

SECTION VI

HARDWARE PROJECTS FABRICATED TO TEST OPERATIONAL PERFORMANCE OF CAD/CAM CAPABILITY

From time to time in this project it is necessary to review the level of development which has been achieved in several fundamental technologies, and the degree to which these technologies function synergistically. We verify new packaging designs, new board designs, improved interconnect techologies, and advances in computer aided design through the fabrication of a small processor which incorporates all of the technologies to be benchmarked. In previous reports, we have described the fabrication of small processors which were intended primarily to test new boards and interconnect technologies; this year, two major and several minor fabrication projects were undertaken, all of which were intended to verify new capabilities in Mayo's computer aided design software.

The two major projects are of particular interest because they demonstrate that the use of computer aided design techniques can yield processors with very high performance, which can be designed, fabricated, and tested in very short durations. These projects will be described in this section. The second of these projects, the fabrication of a small ring communications network originally designed on contract from the U.S. Army, also

demonstrates the synergism which has occurred between the work carried out for this research contract over the past three years and in other contracts sponsoring related work.

Design and Fabrication of A Pipelined Convolver/Correlator

By early July, 1981, the development of Mayo's computer aided design package had reached a level at which several new CAD software features required verification. The first of these new software modules gave us the capability to "CAD" a design using transmission line interconnects for high-speed ECL components, and then to produce a numerical control tape for a semi-automated wirewrap machine. Based upon a review of prior fabrication projects, more than 95% of the residual errors detected in a system which had been CADed but then hand fabricated could be traced to fabrication errors rather than design errors. The provision of a numerical control capability for fabrication of systems using transmission line interconnects was intended to reduce these errors to a considerable extent.

The second module of software to be tested supported computer-assisted system checkout by a technician using a computer terminal to query the CAD data base from which the processor had been fabricated. These software modules permit the technician to perform the checkout rapidly, since the software modules can search the design data base much faster than the

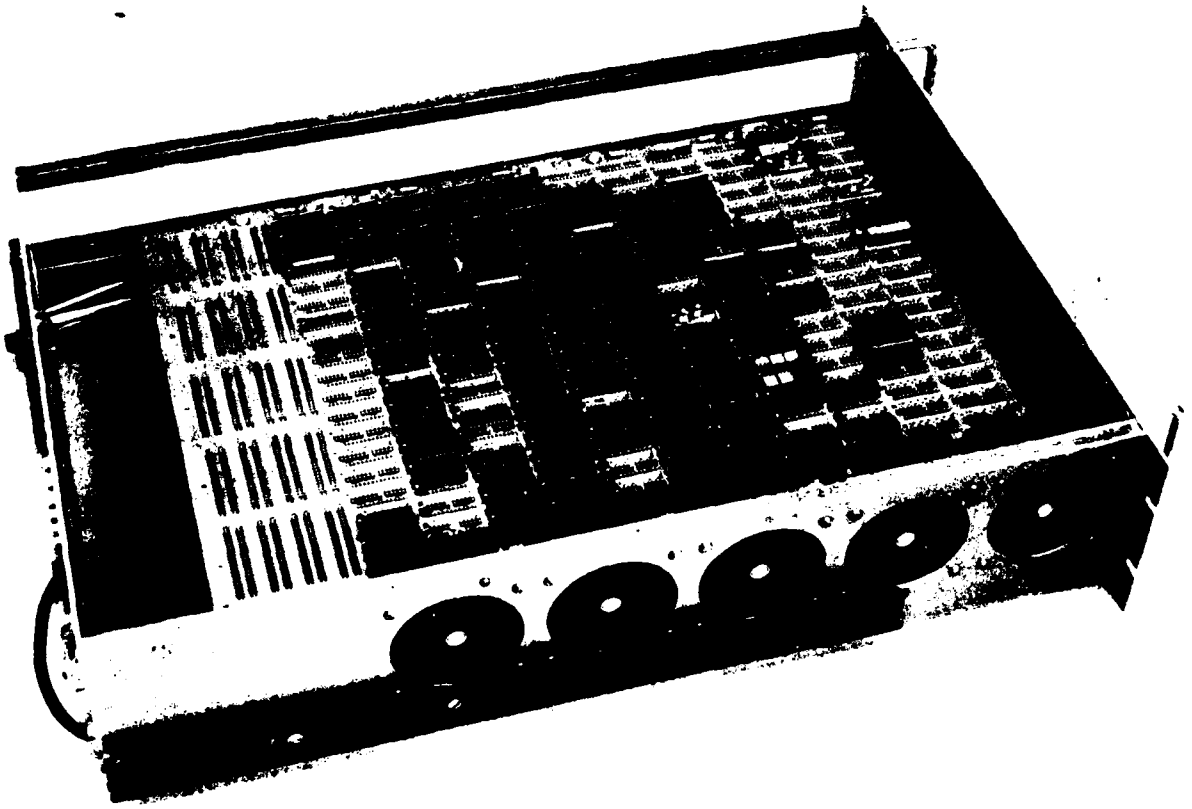
technician can search a set of blueprints. In a prototype development environment, where only one copy of each system is fabricated, fully automatic checkout is not cost effective; rather, manual checkout by a trained technician with the availability of appropriate test equipment and powerful CAD checkout software appears to be a more reasonable approach.

To test these modules, we chose to rework a design described in our previous report, i.e., a high-speed convolver/correlator. Into the original design we incorporated additional pipelining registers, thereby resulting in the maximum feasible speed for this particular structure. Although pipelining had been employed to some extent in the prior version of this convolver/correlator, both horizontal and vertical pipelining were employed in the modified design. Horizontal pipelining indicates that, for example, in a wide-word addition operation, pipelining registers were added between the most and least significant sections of the carry-adder. As a result of this modification, the least significant portion of an addition is conducted during one clock cycle, and the most significant portion of the same addition is completed during the succeeding clock cycle. During each clock cycle, the least significant portion of the adder begins processing the next successive pair of data items.

The original convolver/correlator was redesigned; the addition of horizontal pipeline registers increased the total parts count from approximately 100 integrated circuits to approximately

125 devices. To verify that the computer aided design software could be used by someone unfamiliar with CAD methodology, the incorporation of the pipeline registers into the original design was performed by the designer of the original system by redlining the changes into an earlier set of blueprints; the redlined prints were then given to an engineering summer student who redrew the prints, and then entered all logical design data into the CAD program input data file in a completely random order. The summer student was instructed in the use of the interactive terminal-based computer programs. Using the error diagnostic outputs generated by the CAD programs, the student identified and corrected numerous drafting and typographical errors in the new, fully pipelined design.

To test the CAD system further, the original designer performed a hand placement of the individual components on the logic board, while the student, using the automatic placement algorithms in the CAD, executed an automated placement run of the components in this circuit. The automated placement was about 24% less optimum than the skilled manual placement. After automated placement, the summer student carried the program through an automated optimization phase, and transmission line layout verification. Thereafter, a numerical control tape was prepared for the semi-automated wirewrap machine, and the board, containing approximately 7000 wires, was assembled (Figure 70).



FULLY PIPELINED CONVOLVER-CORRELATOR PROCESSOR DESIGNED AND FABRICATED WITH THE ASSISTANCE OF CAD/CAM.

FIGURE 70

The fabrication duration of five working days was substantially less than the three to four weeks required in previous designs of equivalent size using completely manual construction.

The speed with which checkout preceded was beyond our expectations. Using the recently developed semi-automated software checkout capabilities, the entire system was checkout out and

completely operational in 2½ working days. This duration compares favorably with checkout periods of two to three months for manually assembled systems of equivalent size. The testing proceeded so rapidly because only three faults were detected, all of which were nicked, short circuited, or broken wires; no wires were incorrectly installed. In previous projects, incorrectly installed wires accounted for more than 90% of the errors detected.

Figures 71 and 72 are recordings from the fully operational system on the third day after the initial application of power to the circuit. In Figure 71 risetimes and falltimes are 600 psec and 800 psec respectively. The output from the least significant bit of one of the pipeline data registers (the bit which toggles most rapidly in that register), the output from the least significant bit of one of the binary multiplier/shift networks, the output from one of the adder components, and finally, an output bit from the final stage of the convolver, are all depicted in this figure; note the low levels of system noise. The letters "R" in the middle two panels indicate secondary reflections typical of the parasitic shunt capacitances of the dual inline package inputs, as described previously.

The greatest system clock rate at which the full operation of the convolver/correlator could be assured was 143 MHz, with 6-bit input data and 18-bit output data. At this clock rate, the convolver/correlator generated 1.2 billion additions and 600

DIRECT CONVOLUTION FILTER PROCESSOR
FABRICATED WITH SUBNANOSECOND ECL

(143 MHz System Clock; 6-Bit Input and 18-Bit Output Data; 9 Elements; Wire Wrap Interconnects)

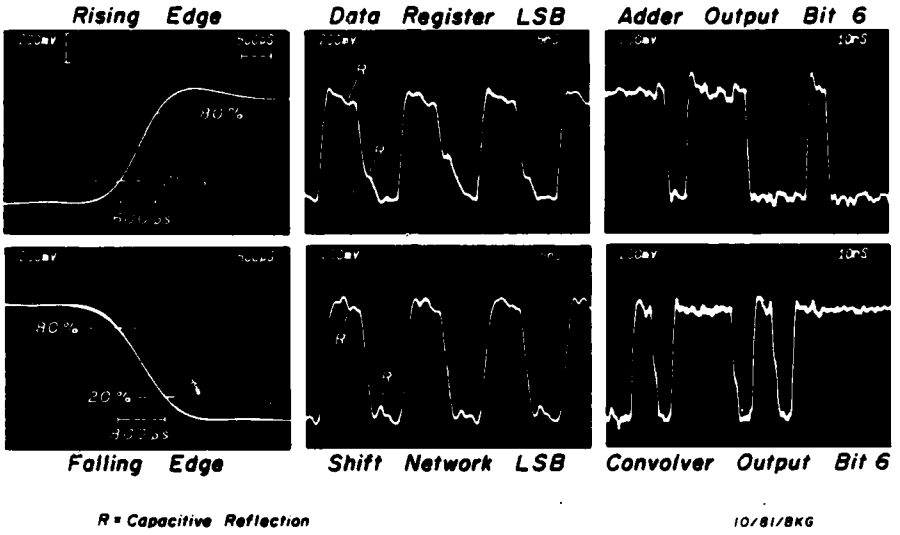


FIGURE 71

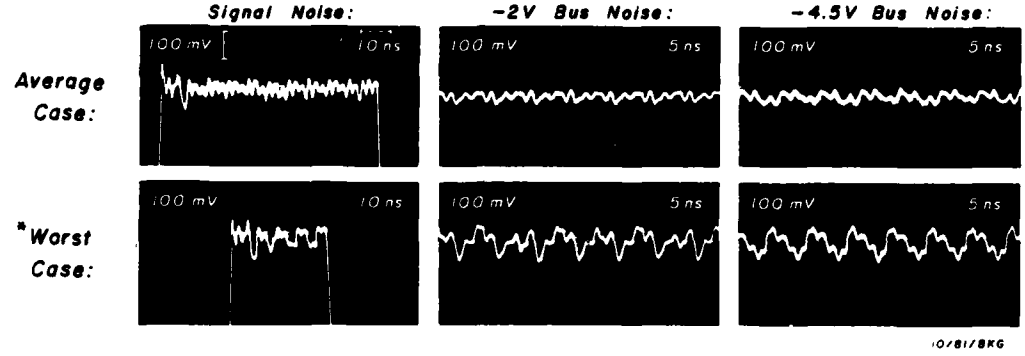
million binary multiplications each second, for a total capability of 1.8 billion special purpose arithmetic operations per second. In Figure 72 the noise curves measured from this circuit indicate that the composite "average case" noise on the individual signal lines is approximately 50 mV peak-to-peak.

The lower row of panels in Figure 72 are worst case noise measurements; however, to generate this much noise, it was necessary to wire a special area of the board in which a signal

string was wrapped onto an intermediate set of pins on a socket which contained no integrated circuit, and from which the decoupling capacitors had been deliberately removed. An area wired in this manner would violate the CAD design rules, and would never be permitted by the CAD program; that is, the worst case noise can be generated only by violating the design rules. Noise amplitudes of approximately 100 millivolts peak-to-peak were observed on the signal traces, on the -2 volt bus, and on the -4.5 volt bus.

DIRECT CONVOLUTION FILTER PROCESSOR FABRICATED WITH SUBNANOSECOND ECL

(143 MHz System Clock; 6-Bit Input and 18-Bit Output Data; 9 Elements; Wire Wrap Interconnects)



*Measured at Empty Socket, with No Decoupling

FIGURE 72

In summary, this set of tests verified that the CAD module which produced the numerical control tape, and the semi-automated CAD checkout software module, both operated properly, resulting in extremely rapid design, fabrication, and checkout of nearly error-free systems. Further, these systems operated at clock rates heretofore difficult to achieve. Incidently, the 143 MHz clock rate observed in this system represents a maximum useful upper bound for subnanosecond ECL components packaged in dual inline packages; higher performance is expected for similar components packaged in improved leadless ceramic chip carriers with accompanying specially designed circuit boards.

Fabrication of a Small Five-Node ECL Ring Communications Network

The second fabrication project undertaken during the past year was also intended to verify a new module of CAD software. By October, 1981, software development of a so-called "hardware macro" capability had progressed to the point at which a test of the software was required. The macro capability allows the designer to develop a "module" of hardware composed of many smaller integrated circuits, then to place this newly designed "super component" in the component library and refer to it by a unique part number. When it is desired to use this "super component" at a later time, the designer retrieves the module from the library and inserts it into the design in progress.

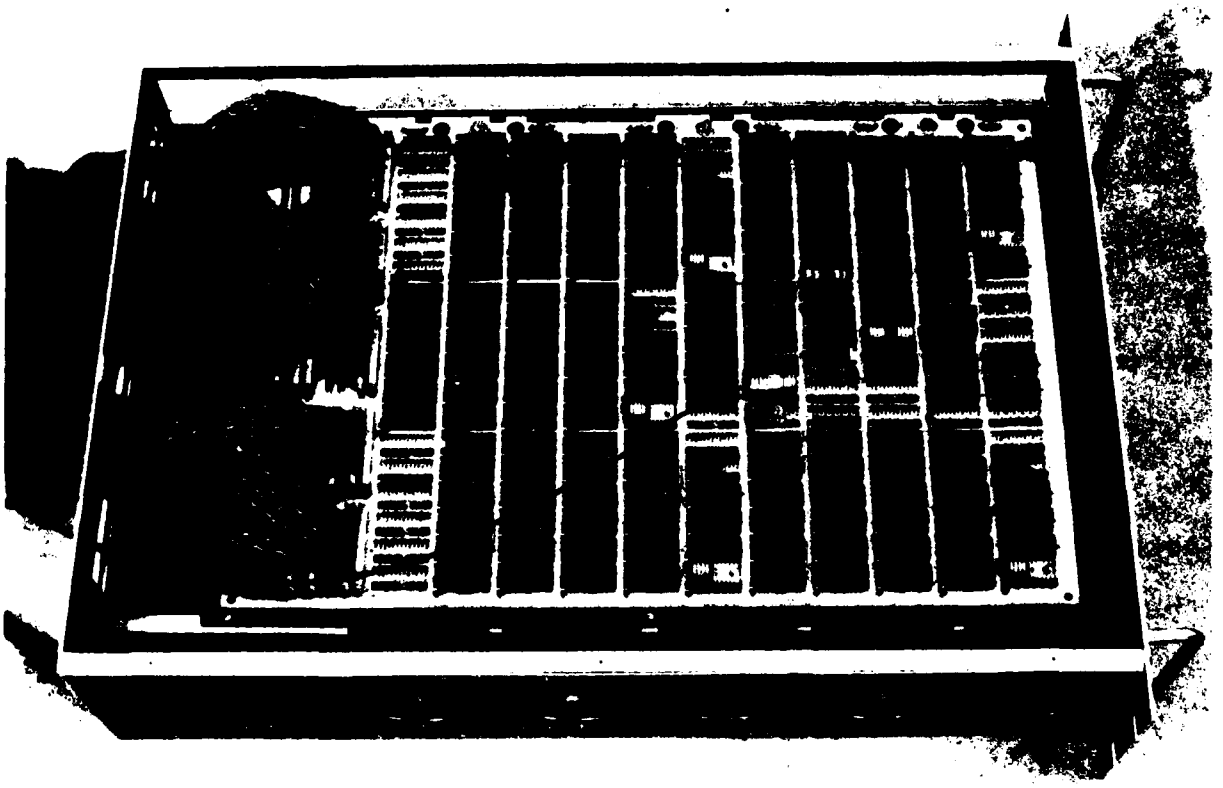
A project has been under way for several years in this laboratory to develop a communications network between cooperating co-processors; the structure is called a "ring" network. All communications "nodes" in the ring are identical; however, to test the ring concept, it was necessary to fabricate and interconnect from three to six identical nodes. It appeared that two benefits could accrue from a fabrication of a small ring network using Mayo's computer aided design capabilities; first, the feasibility of the high-speed ring network could be demonstrated; in addition, we could verify the correct operation of the CAD software macro capability.

Five separate but quite similar nodes were fabricated on the same large circuit board. The logical interconnects of the separate components within each node were identical; however, the physical placement of the individual components within each node differed somewhat because of space considerations on the logic board. This latter set of constraints presented the opportunity to verify the logical interconnect support function of the macro software, and also the ability of the macro software to lay out the hardware components physically in a variety of configurations. To generate the most comprehensive test, each node was handled in a somewhat different manner.

A single ring node was configured using the logical interconnect CAD options; the components employed and the logical interconnections were then defined as a hardware macro. Two of

the five nodes were then subjected to complete auto placement and auto routing using these newly installed features available in the CAD software; in the third through fifth nodes, placement was performed manually, with the final optimized wire routing performed by the automatic software. Following the CADing of the design, the board was fabricated with the automated equipment described earlier.

Figure 73 is a surface view of the circuit board containing the five ring nodes; the single black wire is the coaxial cable

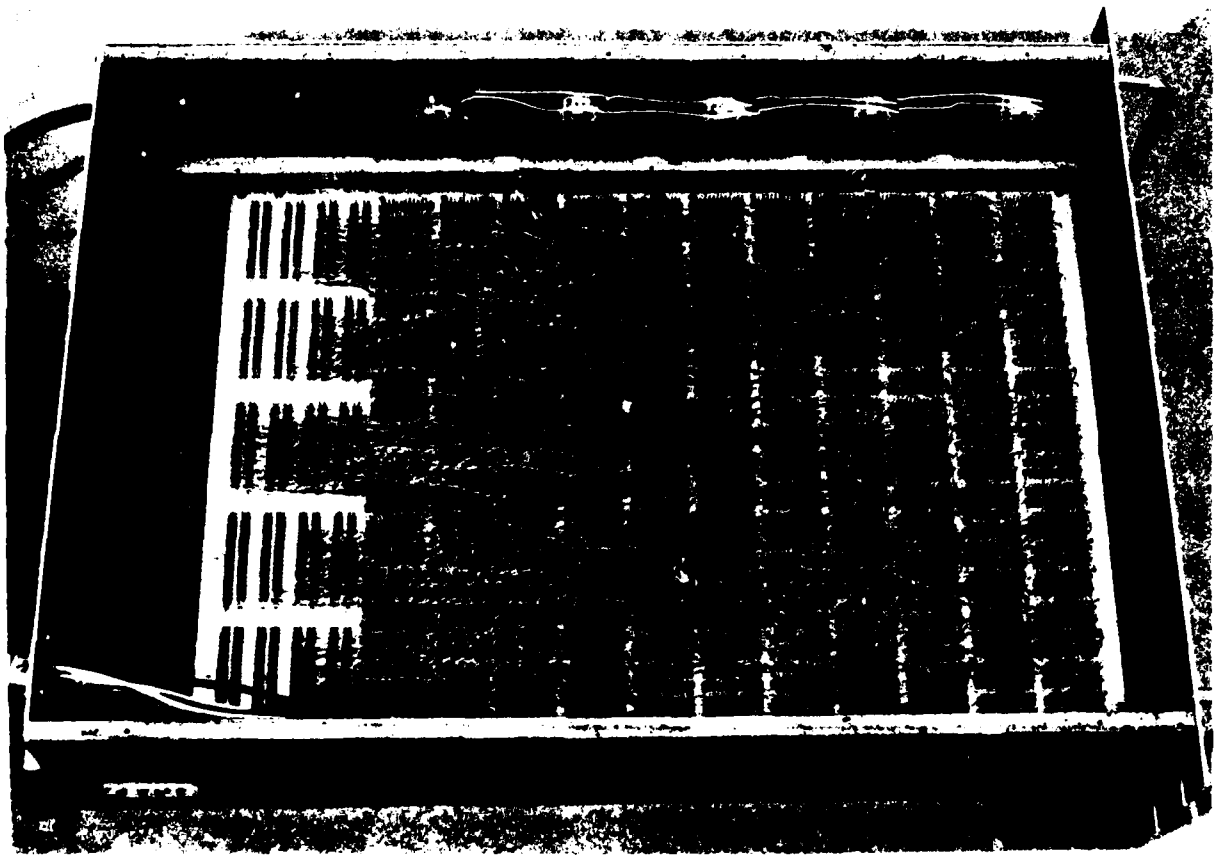


EXPERIMENTAL FIVE NODE RING COMMUNICATIONS NETWORK. A COMMON CLOCK DRIVE AND FANOUT SYSTEM WAS EMPLOYED FOR ALL FIVE NODES, AND IS INCLUDED ON THIS LOGIC PANEL.

FIGURE 73

which supplies the system clock to all five ring nodes. The braided cables at the left of the board are the interconnects which transfer data from one node to the next; to add realism to this test, the inputs of the five individual nodes were derived from these board connectors, and their outputs were fed to connectors. Since in a full scale ring system a single large node would occupy one complete logic board, this approach to the test system fabrication correctly duplicated the effects of cable delays between elements of a full scale system. The small DIP switch components at various locations on the board were also placed by the CAD program, demonstrating the ability of the CAD to handle nonstandard components. Descriptions of these specialized components are included in the component library along with the logic and memory devices.

Figure 74 is a photograph of the wirewrap surface of the board, showing the uniform distribution of the wiring, and the twisted pair feeds from the five nodes to the cable connectors. Figure 75 is an expanded photograph of the component surface of the board; again, note the variety of component types which were placed, routed, and wired with the CAD program. The coaxial cable supply for the external clock source enters the board from the upper left corner of the figure, and terminates on a special coaxial cable adapter. The composite clock drive circuitry for all five nodes was also fabricated on the board, and driven from the coaxial clock line.



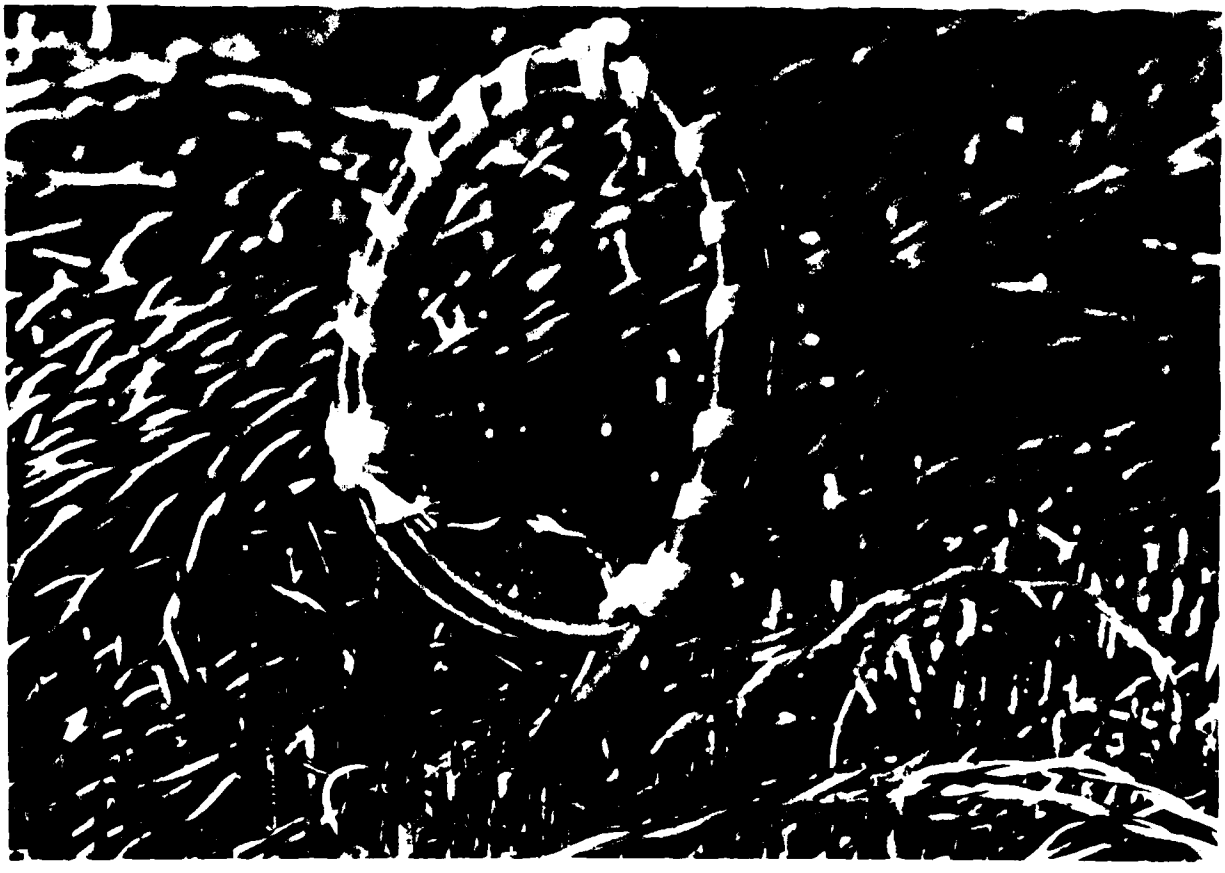
WIRE-WRAP SIDE OF EXPERIMENTAL COMMUNICATIONS NETWORK. ALL WIRES WERE INSTALLED WITH NUMERICALLY CONTROLLED WIRE-WRAP MACHINE

FIGURE 74

DETAIL VIEW OF COMMON CLOCK CIRCUITRY AND ONE NODE OF EXPERIMENTAL COMMUNICATIONS NETWORK.

FIGURE 75

Figure 76 is a photomicrograph of a fixed duration delay element which was incorporated into the design of each node; a short length of coaxial cable was employed rather than an active delay because better time stability could be achieved with the cable. The coaxial delay was also correctly accommodated by the CAD program.



PHOTOMICROGRAPH OF DELAY ELEMENT USED AS A TIMING TERM IN THE DESIGN OF COMMUNICATIONS NETWORK NODE. CAD CORRECTLY ACCOMMODATED THIS DELAY ELEMENT.

FIGURE 76

General Description of Ring Network

Before presenting performance data from this system, the design and operation of the five-node ring network will be discussed briefly. A "ring" network can be visualized as a series of M-bit registers, with the Q outputs of the I^{th} register connected to the D inputs of the $(I+1)^{st}$ register, and so on

DATA FLOW PATHS IN EXPERIMENTAL FIVE NODE RING COMMUNICATIONS NETWORK FABRICATED WITH SUBNANOSECOND ECL

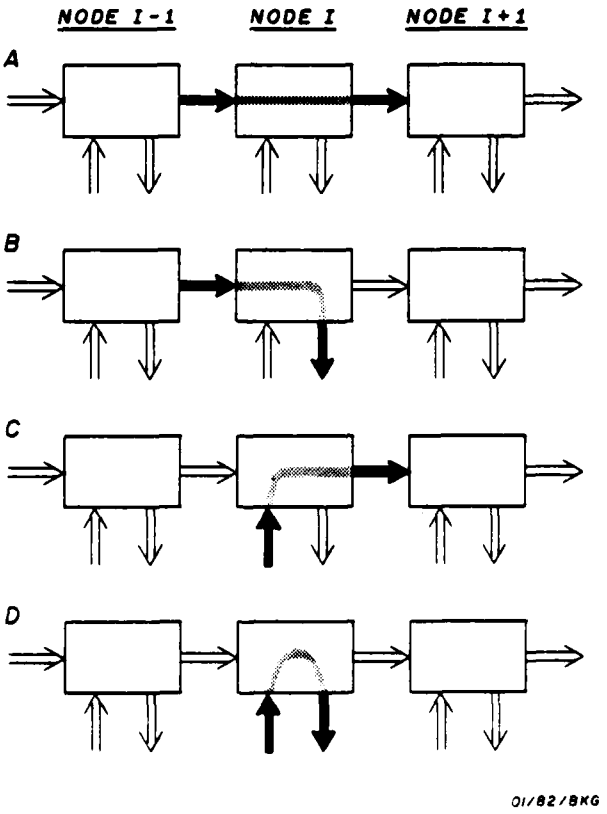


FIGURE 77

until the Q outputs from the N^{th} register are connected to the D inputs of the first register. Hence, if the N individual registers are visualized as being placed on end in a vertical configuration, the overall structure can be visualized as the surface of a hollow open-ended tube. During operation, all of the individual D-type registers are clocked simultaneously and continuously, forcing the contents of each register to be transferred to the next successive register; a data value present in the I^{th} register will be clocked into the $(I+1)^{st}$ register, then into the $(I+2)^{nd}$ register, and finally, into the N^{th} register, and thereafter into the first register, and so on. In addition, the inputs and outputs of each register in the N-register loop are made accessable to an external device, which can read one or more data words from its associated register (hereafter called the "local ring register") as the data words spin by on the surface of the ring; the external device also can place data words on the surface of the ring by inserting them into the inputs of its local ring register (see Figure 77).

The contents of any given ring register are referred to as a "data item." The bits within each data item are assigned to one of three separate functions: 1) to the operands undergoing transfer on the ring; 2) as memory addresses for a given memory module; and 3) as specific control and "node address" information to and from the processing and memory elements. A device such as a processing element, attempting to send data to another element on the ring, configures a data item containing the operand to be

transferred and a destination node address for this information (i.e., the address of one of the memory or processing elements served by the ring). When an unused "data item slot" passes by on the surface of the ring, the data item is "injected" into the local ring register (i.e., into the empty slot); it is then rapidly carried away by the "spinning" effect of the ring operation.

Just before the data item enters the "local ring register" dedicated to the addressed destination device, the address bits specifying the destination are decoded by the local ring register bookkeeping logic; if an address match is sensed, the data item is read in its entirety from the surface of the ring during the next interclock interval. Several dedicated control bits in the local ring register (which actually form part of the node address field) are then reset, thereby releasing that "slot" on the rotating surface of the ring for another data item transaction. Note that the source device merely places its data item onto the surface of the ring in the first available empty slot, and need not establish specialized links to assure that the destination device will receive the data item. The design of this interconnect network is also synchronous, and in fact is completely self-synchronizing. We have proposed for several years that the excessive propagation delays typical of such a ring network can be avoided by the use of high-speed digital components, e.g., subnanosecond ECL, in its fabrication.

The prototype communications ring network assembled for this test is a 12-bit wide design which provides a communications link for up to five devices. The ring network allows any device to send data to and receive data from any other device, with all operations being performed simultaneously. Each of the five nodes may be interfaced with one external device, with the device access to the ring controlled by the node. The prototype network was fabricated with subnanosecond ECL components packaged in 24-pin ceramic dual inline packages.

Preliminary Operational Results

The overall ring system clock rate is determined by the longest node-to-node wire pathway, which in this system is four feet. This length includes one foot of woven, twisted cable and three feet of on-board interconnect wire. A system clock rate of 55 MHz, i.e., an interclock interval of 18.2 nsec, was achieved (Figures 78, 79, and 80). At 1.5 nsec of propagation delay per foot of wire, the 18.2 nsec interclock interval contains a 7 nsec contribution from the interconnects. Hence, the logic speed of the nodes themselves was computed as approximately 82 MHz. System noise levels are quite similar to those observed in other processors fabricated at Mayo; the circuit maintains a satisfactory noise margin which should make it quite resistant to spurious glitches and noise spikes.

OPERATION OF FIVE NODE RING COMMUNICATIONS NETWORK FABRICATED WITH SUBNANOSECOND ECL

(55 MHz Clock; 18.2 ns Period; 4 Foot Internode Separation; CERDIP Encapsulation)

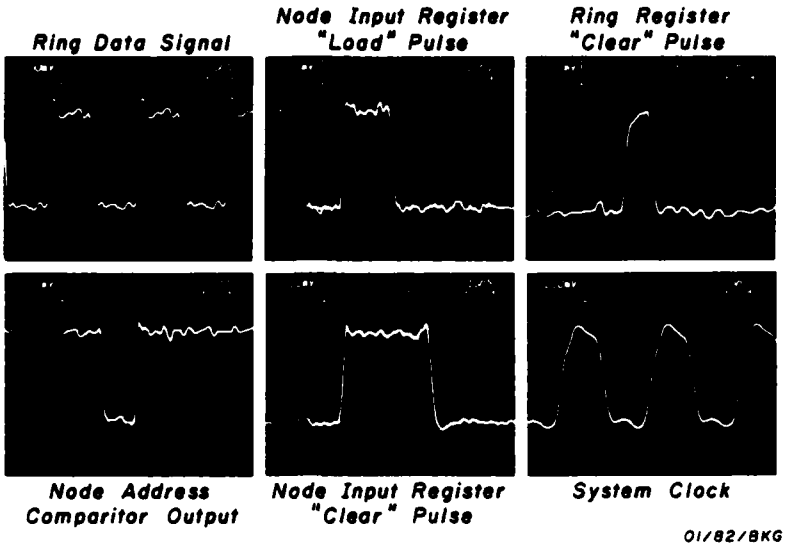
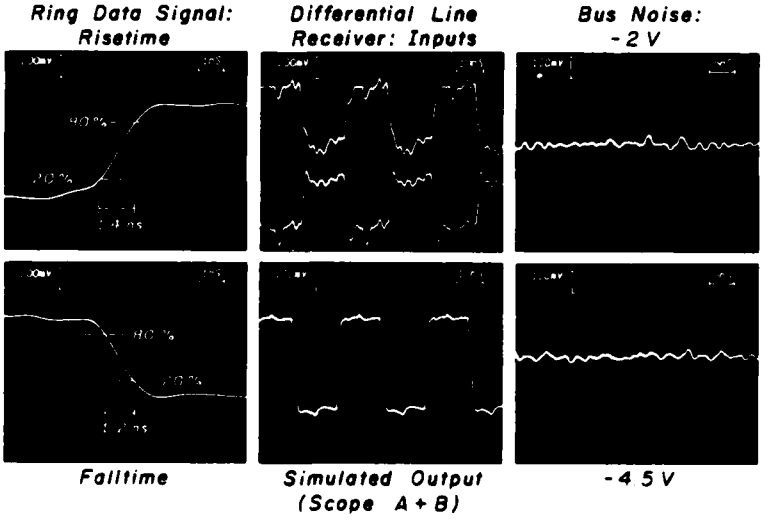


FIGURE 78

OPERATION OF FIVE NODE RING COMMUNICATIONS NETWORK FABRICATED WITH SUBNANOSECOND ECL

(55 MHz Clock; 18.2 ns Period; 4 Foot Internode Separation; CERDIP Encapsulation)



OPERATION OF FIVE NODE RING COMMUNICATIONS NETWORK FABRICATED WITH SUBNANOSECOND ECL

(55 MHz Clock; 18.2 ns Period; 4 Foot Internode Separation; CERDIP Encapsulation)

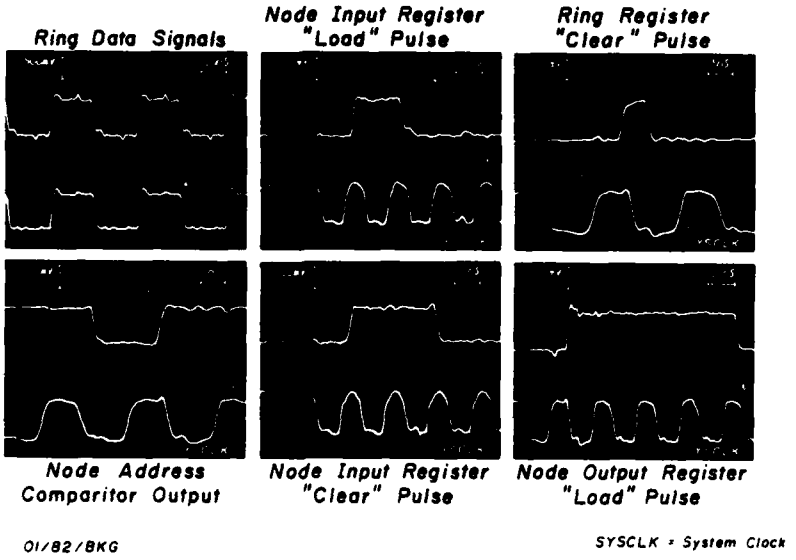


FIGURE 80

The simplicity of such a system is illustrated by the fact that the recently completely prototype 5-node ring network required a total of less than 200 integrated circuits, including line drivers, line receivers, control logic, all registers, and DIP-switches; thus, a very high level of performance, which would not be achievable with alternative network structures, was realized with an extremely small package count. In addition, the correct operation of the network validated the software enhancements to the Mayo CAD package.

SECTION VII

INITIAL TESTS OF INTEROPERABILITY BETWEEN EMITTER COUPLED LOGIC AND GALLIUM ARSENIDE INTEGRATED CIRCUITS: CHIP CARRIER AND LOGIC BOARD COMPATIBILITY

The problems of high frequency system design, logic board layout, component packaging and interconnect technology investigated in this research project during the past three years are clearly not limited to high-speed emitter coupled logic. A device technology in which the system gate propagation delays are (much) less than 1 nsec should possess offchip signal risetimes of approximately the same duration. Slow offchip risetimes are the second major contributor to long interchip propagation delays; long interconnects, which are normally indicted as the major contributor to this problem, are in fact only half of the difficulty. The difference between a signal risetime of 1 nsec and one of 200 psec is equivalent to six inches of wire between two components. Hence, it is not sufficient to assure compact component layouts with minimum interconnect lengths, if the time saved by the high packing density is dissipated by long risetimes of a nanosecond or more.

The research under way in this project in computer aided design, layout, packaging, and interconnect technology is creating a generic set of capabilities which can be applied to

any high speed component family. Thus it seemed appropriate to examine the system implications of Gallium Arsenide integrated circuits, now in early stages of development in several laboratories, since these new components have already demonstrated offchip risetimes in the range of 300 psec or less, and gate propagation delays in the 75-200 psec range. Components with these performance characteristics can be expected to stress the packaging and interconnect technologies under development at Mayo, and hence should provide additional data regarding the efficacy of our solutions to these challenges.

In collaboration with Rockwell International Microelectronics Research and Development Center, Thousand Oaks, California, we acquired a number of Gallium Arsenide digital devices based upon the Schottky-diode FET Logic (SDFL) structure pioneered by Rockwell. These components were packaged in commercially available leadless chip carriers and ceramic flat packs, and were then tested in a variety of interconnect configurations in operating brassboard circuits. The components tested to date are of two distinctly different design generations. The first of these, represented by "divide-by-40/41, 80/82" prescalers, were designed in 1978, using early design rules and one inch diameter wafers characteristic of Gallium Arsenide crystals grown by the Bridgeman technique. The second set of components, represented by "divide-by-4" and "divide-by-16" counters, were fabricated using recent design and layout rules on crystal substrates grown by the Liquid Encapsulated Czochralski (LEC) technique.

Figure 81 shows the measured results recorded directly (with a wideband 1 GHz oscilloscope) of a divide-by-40/41 counter packaged in a small commercially available 24-pad leadless chip carrier. The packaged counter was vapor phase reflow soldered to a multilayer circuit board, and driven with a sign wave clock operating at a variety of frequencies. Note the 250 psec signal risetime, and the correct operation of the divide-by-41 output at

BOARD-LEVEL PERFORMANCE OF
SDFL GALLIUM ARSENIDE INTEGRATED CIRCUIT
ENCAPSULATED IN COMMERCIAL LEADLESS CHIP CARRIER
UNDER VARIOUS OPERATING CONDITIONS
(Component: ÷ 40/41, 80/82 Prescaler;
LCCC Vapor Soldered to PC Board)

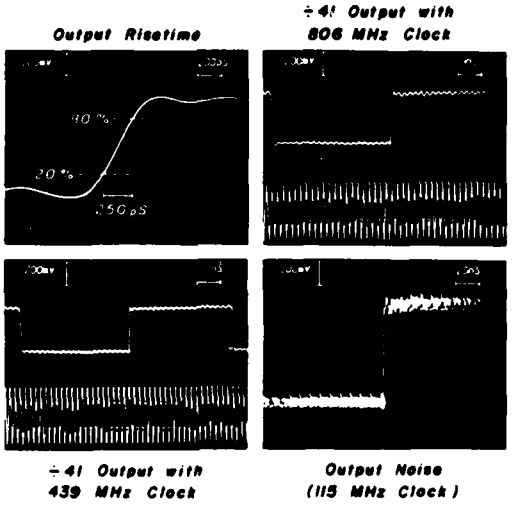


FIGURE 81

439 MHz and at 806 MHz clock input frequencies. The output noise displayed in the lower right panel is higher than desirable for a large operational system, but is acceptable considering the non-optimum nature of the circuit board and commercial chip carrier used in this early test.

One of the notable features of this early integrated circuit was its sensitivity to supply voltage variations. Each component required a unique combination of power supply voltages, and would function properly only when these voltages were within 10 to 20 mV of the nominal for that specific component. Power supply voltage sensitivity of this magnitude would obviate the use of such integrated circuits in a large system design.

Conversely, Figure 82 depicts measurements recorded from a recent Gallium Arsenide integrated circuit fabricated with new design rules and materials; these components were installed in 16-pin leaded flat packs and operated at a maximum sine wave input clock frequency of almost 2.5 GHz. Neither the leaded flat packs nor the circuit board were optimized for these components. All interconnects between circuits, and between chip outputs and their terminators, were wire wrapped. The two leftmost panels display signal risetimes on the output of the divide-by-four counter of 320 psec using direct oscilloscope measurement, and 300 psec using a 3½ GHz passive logic probe and Tektronix 14 GHz S-4 sampling heads. The close agreement between the risetimes

OPERATION OF SDFL GALLIUM ARSENIDE
DIVIDE-BY-4 COMPONENT IN CIRCUIT BOARD ENVIRONMENT
(2.47 GHz Sine Wave Clock;
16-Pin Leaded Flat Pack; Wire Wrap Interconnects)

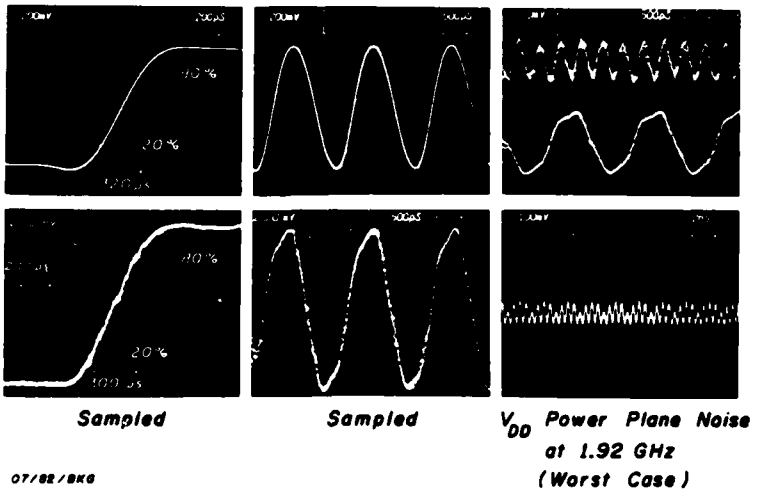


FIGURE 82

from the sampled and direct measurements implies that the wide-band oscilloscope contributes very little dispersion to the signal edges.

In the upper and lower middle panels, the direct and sampled measurements display a 1200 millivolt peak-to-peak signal swing; although there is some evidence of reflections from package parasitic shunt capacitances, there is otherwise very little waveform distortion. A sampled comparison between the clock input and the divide-by-four output appears in the upper right panel of Figure

82. The V_{DD} power plane displays a worst-case amplitude noise level (at 1.92 GHz) of 100 mV peak-to-peak for this non-optimized circuit board.

Figure 83 depicts operational measurements from a small circuit composed of three Gallium Arsenide divide-by-four counters in a single cource, dual destination signal string arrangement. At a sine wave input clock frequency of 2.07 GHz, the rise and fall times of the driving gate, as determined from sampling measurements, are 270 psec and 300 psec respectively. The

OPERATION OF SDFL GaAs
DIVIDE-BY-4 COMPONENTS IN
SINGLE-SOURCE, DUAL DESTINATION SIGNAL STRING
(2.07 GHz Sine Wave Clock Drive;
Flat Pack/LCCC Encapsulation;
Wire Wrap Connections)

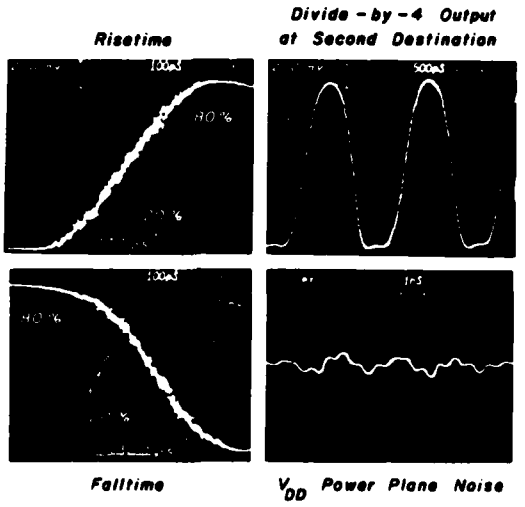


FIGURE 83

conformation of the driving waveform is of high quality, is free of secondary reflections, and of about 1300 mV amplitude peak-to-peak. The lower right panel in this figure depicts a V_{DD} power plane noise voltage waveform of approximately 100 mV peak-to-peak. Although the output impedance of the driver transistor in the source gate is higher than optimum, and the input impedances to the two destination components are lower than optimum as a result of the SDFL configuration, the drive characteristics of the output transistors are sufficient for high frequency communication between multiple components. All components in this circuit were packaged in 16-pin Mini-Systems flat packs, the impedance characteristics of which are presented in Figure 3.

To verify that the measurement of these circuits with 3.5 GHz passive probes and a wideband direct oscilloscope are of sufficient fidelity, a sine wave clock input and the outputs of a divide-by-four counter were measured first with the direct technique, and then, with the same probes, using a pair of Tektronix S-4 14 GHz sampling plug-in units. The results of these two sets of measurements appear side-by-side in Figure 84. The amplitude of the 1.89 GHz sine wave clock input, nominally one volt peak-to-peak, appears in the direct measurement to be less than 500 mV in amplitude, and with a slower oscillation imposed upon it. The sampling measurement also indicates some slow wave superposition; however, the signal amplitude is one volt peak-to-peak.

OPERATION OF SDFL GALLIUM ARSENIDE
DIVIDE-BY-4 COMPONENT IN CIRCUIT BOARD ENVIRONMENT
(1.89 GHz Sine Wave Clock; 16-Pin Leaded Flat Pack Encapsulation;
Wire Wrap Interconnects)

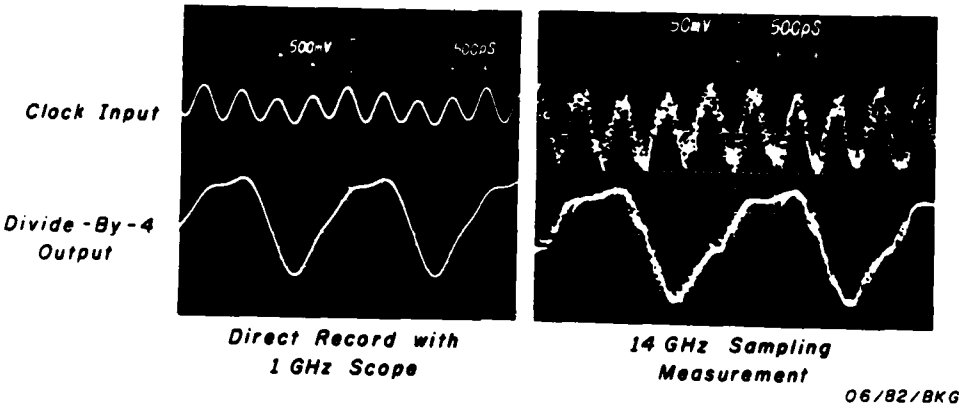


FIGURE 84

Conversely, the divide-by-four outputs, at a frequency of approximately 450 MHz, are comparable in the direct recording and in the sampling measurements. These measurements indicate that, for traces with fundamental frequencies in the 250 MHz-1 GHz range, direct measurements accurately reproduce the waveform; however, above these frequencies, sampling measurements will be required until direct oscilloscopes with wider bandwidth become available.

Compatibility Between ECL and GaAs Components

For the foreseeable future, the number of available Gallium Arsenide part types will be low enough to preclude the design and fabrication of entire systems based only upon this family of integrated circuits; in addition, interfacing to another logic family at the boundaries of such a system will always be necessary. In a research project sponsored by the Navy, we have attempted to develop techniques for the direct interfacing of Gallium Arsenide and ECL integrated circuits, even though the power supply voltages, logic swings, and risetimes of the two types of logic are completely different. Exploiting the fact that the Gallium Arsenide substrate is semi-insulating, it is possible to electrically isolate the Gallium Arsenide integrated circuit from its chip carrier encapsulation by a modification of the wire bonding process. The nominal GaAs V_{SS} and V_{DD} power supply voltages can then safely be down-converted to levels below ground, thereby achieving almost identical threshold voltages for the GaAs and ECL components, and compatible, though not identical, logic swings.

Figure 85 depicts the operation of an SDFL Gallium Arsenide divide-by-four integrated circuit directly driving one ECL 6-bit D-type register. This figure displays the operation of the small circuit, indicating no missed transitions either for the GaAs or the ECL components, at clock rates of 1 GHz, 1.14 GHz and 1.39 GHz. These three panels depict the sine wave clock input and the

output of the ECL chip, which latter was wired as a divide-by-two counter; an overall divide-by-eight countdown from the sine wave clock input was thus achieved.

However, note the considerable amount of interference of the clock signal with the output traces themselves. This problem was caused by the nonoptimal design of the leaded flat pack encapsulation of the GaAs components and the nonoptimal design of the logic boards used in these studies. The amount of energy leakage from the clock signal into the remainder of the circuit is

OPERATION OF SDFL
GALLIUM ARSENIDE DIVIDE-BY-4 COMPONENT
DIRECTLY DRIVING ONE ECL REGISTER
(Sine Wave Clock Drive; Negatively Shifted GaAs Supply Voltages; 16-Pin Leaded Flat Pack Encapsulation; Wire Wrap Interconnects)

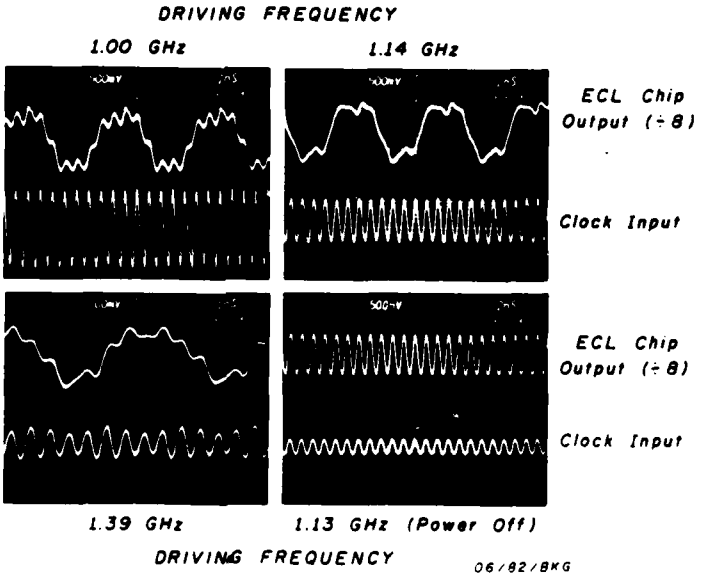


FIGURE 85

apparent in the lower right panel of this figure, in which the clock was operated at a frequency of 1.13 GHz, but the board power was turned off. Clock waveform leakage into the output of the unpowered ECL chip is obvious. Redesign of the encapsulation and board substrates would have removed this problem and improved the conformation of the signals depicted in the remaining panels of this figure. The significant result of this test was the successful identification of a set of compatible operating conditions for Gallium Arsenide and ECL components, in spite of the vast difference in power supply voltages and logic swings for the two families. Although the development of ECL/Gallium Arsenide translator components may be necessary in the future, this matching technique appears to operate well enough that it may be used in larger system designs.

Figure 86 shows results similar to those of Figure 85, but with one Gallium Arsenide component driving two ECL registers wired in a shunt-terminated transmission line interconnect. Note the Gallium Arsenide drive gate risetimes and falltimes of 330 psec and 480 psec respectively; the rather "slow" falltimes are a result of the characteristics of the terminator resistor in this network, which pulls the logic signal from high to low (the GaAs driver transistor drives the signal from low to high). Waveform conformations for the GaAs chip output and for the ECL register output at 1.02 GHz and 1.37 GHz sine wave input clock rates respectively are quite adequate. A small secondary reflection from the shunt capacitances of the chip carrier encapsulation in

which the ECL components were packaged may be observed in the troughs of the curves. The conformation of these signals should be good, since the input impedance to each of the ECL components is approximately 10^{10} ohms; conversely, the input impedance to a typical SDFL gate is 1000 ohms or less, thus placing a substantial load across the transmission line.

OPERATION OF SDFL GALLIUM ARSENIDE DIVIDE-BY-4 COMPONENT DIRECTLY DRIVING TWO ECL REGISTERS

(Sine Wave Clock Drive; Negatively Shifted GaAs Supply Voltages; 16-Pin Leaded Flat Pack Encapsulation; Wire Wrap Interconnects)

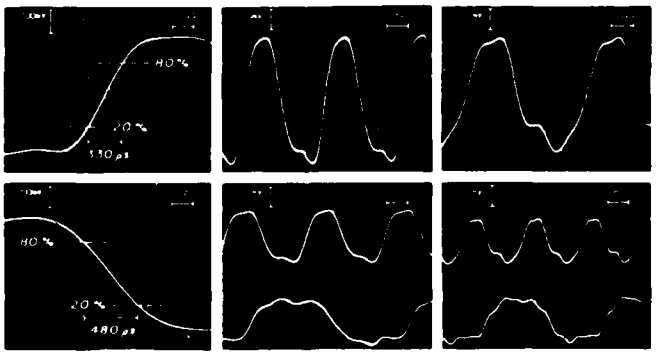


FIGURE 86

OPERATION OF SDFL GaAs DIVIDE-BY-4
AND Si ECL COMPONENTS IN VARIOUS DRIVE COMBINATION
(2.07 GHz Sine Wave Clock Drive; Negatively Shifted GaAs Supply Volta
Flat Pack/LCCC Encapsulation; Wire Wrap Connections)

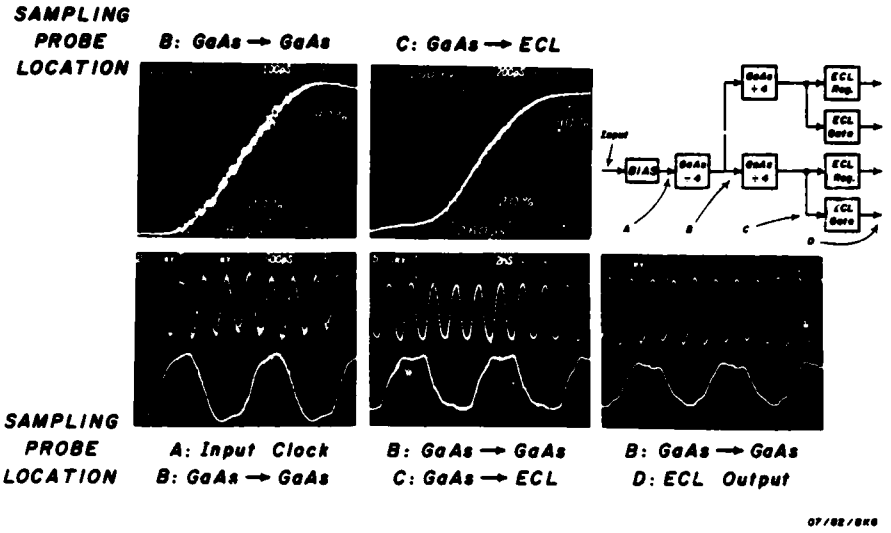


FIGURE 87

Figure 87 depicts the results of a more complex experiment, in which a single GaAs divide-by-four counter was employed to drive two additional GaAs divide-by-four counters operating in parallel; each of these latter GaAs chips in turn drove a pair of ECL components. In all cases, shunt terminated wire wrapped transmission line interconnects were employed. Figure 87 includes a small schematic of the circuit layout which indicates the four locations from which sampling measurements were taken. In the upper two panels, the risetime of one GaAs component driving two GaAs components was approximately 280 psec. When a single GaAs divide-by-four component drove two ECL components, the signal risetime was 260 psec, probably as a result of the high input impedances of the ECL components. The three lower panels of Figure 87 depict measurements of the input clock, the waveform

conformation with a Gallium Arsenide component driving two other Gallium Arsenide components, of Gallium Arsenide components driving ECL devices, and of the ECL output itself. Signal swings and waveform conformations in all cases appear excellent.

Figure 88 presents a series of photographs of the physical layout of the three Gallium Arsenide and four ECL components used in these tests. Because the circuit boards available for these

PHOTOMICROGRAPHS OF BOARD-MOUNTED FUNCTIONING GaAs COMPONENTS: DIFFICULTY OF ACHIEVING GOOD QUALITY GROUNDS IN DIGITAL RF SYSTEMS

(16-Pin, 250 mil² Leaded Flat Packs)

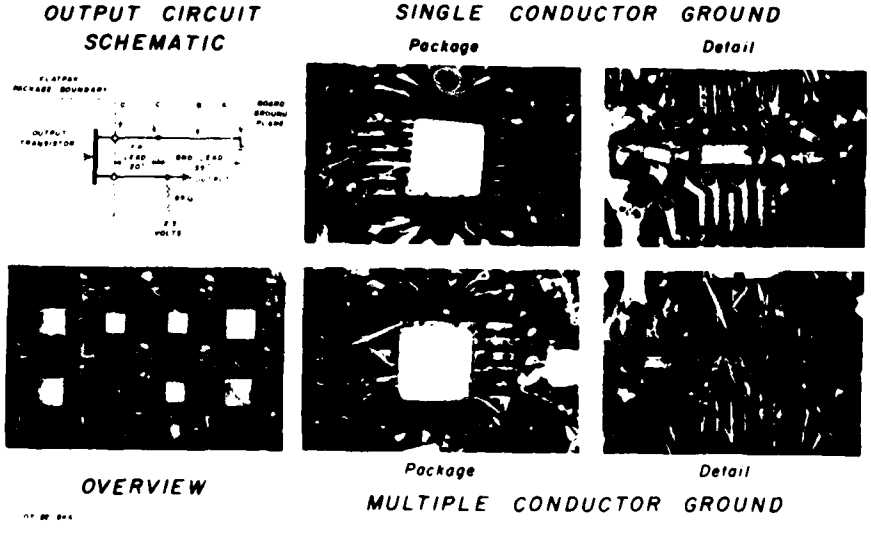


FIGURE 88

tests were not optimized for the flat packs in which the Gallium Arsenide components were encapsulated, it became necessary to cut several board foils and extend others with short wires. Measurements of the operating circuit at high frequencies led to several interesting conslusions. In the upper left corner of this figure a small schematic has been included of the output driver in its flat pack encapsulation, as well as the electrical circuitry driven by this GaAs FET transistor.

The driver transistor was connected in a source follower-to-shunt terminated transmission line arrangement, with a termination resistor value of 85 ohms (75 ohms impedance). The transistor drain leg should nominally be clamped to ground to maintain a low noise level on the signal line. However, the board was not designed for this application; the ribbon lead from the flat pack was extended .2 inches from the edge of the ceramic flat pack (labeled point D) to a convenient metal land on the circuit board (labeled point C), and thereafter through either a single or a multiple ground lead .35 inches in length to the board ground plane itself. Hence, the total wire run length for the ground lead was .55 inches. Both cases, i.e., in which a single ground from point C to point A was used, and in which a multiple-wire ground was installed to decrease series inductance, are depicted in the upper row and the two lower right panels of Figure 88 respectively. Test points A through D are also labeled

in the upper right and lower right panels. The circuits were operated under a variety of conditions, i.e., with ECL components driving Gallium Arsenide components, and with Gallium Arsenide components driving ECL components.

Figure 89 shows noise levels on the ground plane of the board (point A), and at points B, C, and D between the ground plane and the entry of the ribbon tie into the leaded flat pack

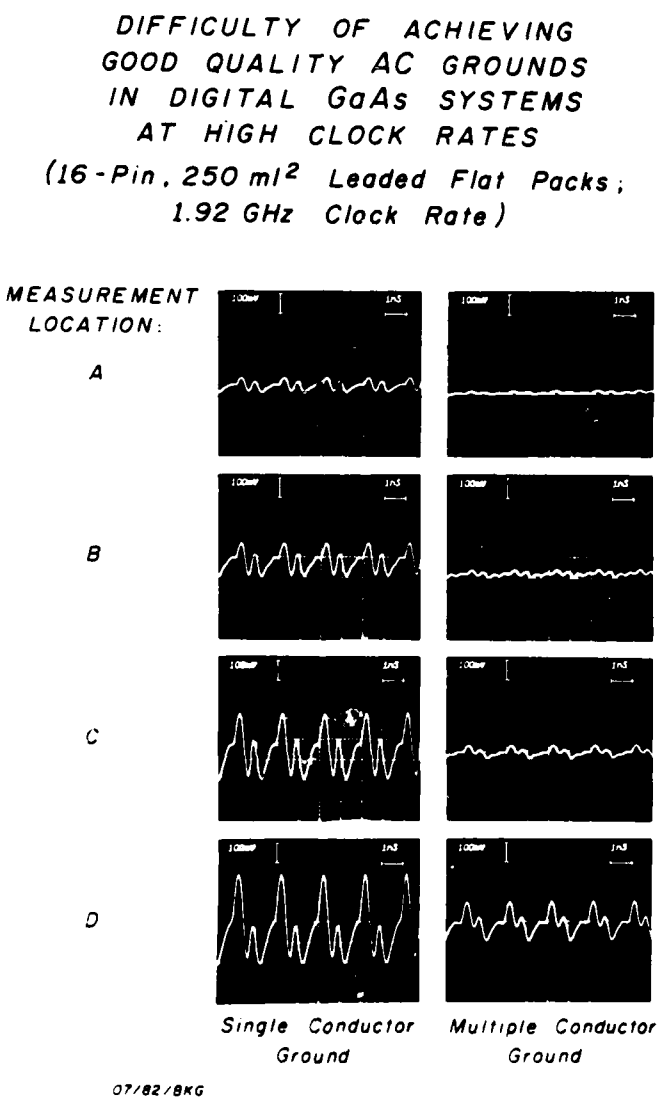


FIGURE 89

of a Gallium Arsenide component. Both a single conductor ground strip, and a multiple conductor ground strip composed of three separate wire leads, were measured and are presented in this figure. In the left column of panels, for the single conductor ground, the noise at the ground plane is almost 100 mV peak-to-peak, increases steadily as the grounded end of the flat pack ribbon lead is approached, and increases further at the entry point of the ribbon into the ceramic body of the flat pack (point D). Noise voltages on the ground pin increase from 200 mV peak-to-peak at point B to more than 400 mV peak-to-peak at point D. The right column of panels in this figure shows similar measurements recorded with a multiple conductor ground between points C and A. Noise voltages at points A and B are 20 mV and 40 mV respectively, but increase to 80 mV at point C and 200 mV at point D.

The right column of panels thus indicates that the .2 inch length of ribbon conductor from the leaded flat pack to its ground point on the printed circuit board contains sufficient inductance (2 nH) to cause substantial inductively generated noise on the ground reference of the driver transistor. This lead inductance renders it impossible to achieve high quality AC grounds and a low noise AC environment for integrated circuits whose output risetimes contain harmonic components of 2 GHz and above.

Even though the integrated circuits in these tests may appear to operate correctly, their noise margins can be significantly degraded by such inductively generated noise sources, whether in leaded flat packs or leadless ceramic chip carriers. Figure 90 shows measurements from an ECL component driving a pair of GaAs SDFL components. The two rightmost panels in this figure display the ECL gate output and the output of the GaAs divide-by-four counter at sine wave input clock frequencies of 126 MHz and 411 MHz respectively. Note the high noise level on the GaAs divide-by-four output; this component was packaged in a leaded flat pack with .2 inch ribbon ties to the board ground plane. Although the circuits operate correctly with no missed transitions, the system noise margin is compromised by the behavior of the AC power buses themselves.

This noise background is apparent in the differential measurements of noise on the ground pins of the flat pack-encapsulated Gallium Arsenide integrated circuits; in the upper right panel of Figure 87, only a single connection was made between the leaded flat pack ground lead and the board ground bus (referred to in this figure as a "ribbon tie"). Note the sharp ringing behavior of this signal, which corresponds temporally to the occurrance of a switching transition in the Gallium Arsenide components. Closer observation shows that there are in fact two ringing phenomena, the first occurring at the rising edge and the

OPERATION OF Si ECL COMPONENT DRIVING
SDFL GaAs COMPONENT IN CIRCUIT BOARD ENVIRONMENT
(Flat-Pack/LCCC Encapsulation;
Negatively Shifted GaAs Supply Voltage; Wire Wrap Connections)

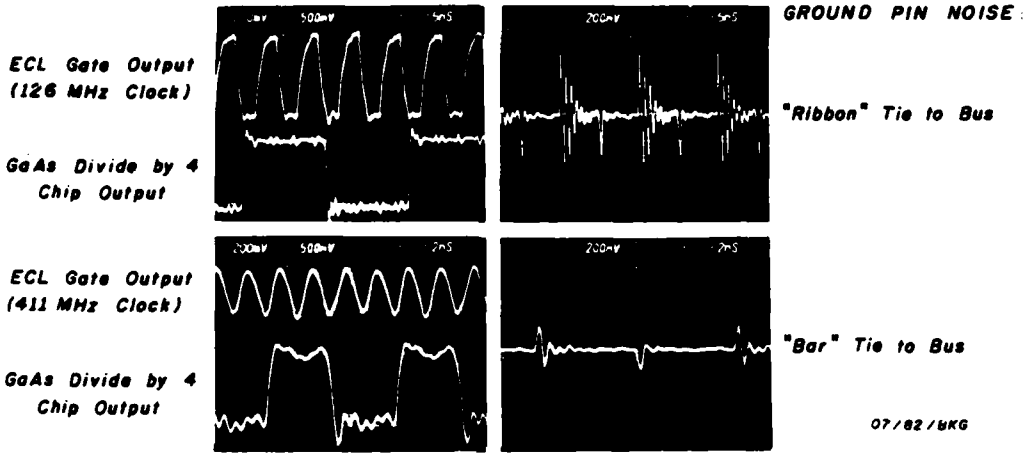


FIGURE 90

second at the falling edge of the ECL gate drive, with the predominant noise at the rising edge. Both of these ringing spikes occur when the internal logic in the divide-by-four counter

switches states. In the lower right panel of Figure 90, the ribbon feed from the ground pin of the GaAs component packaged in a leaded flat pack was made substantially heavier with the addition of small parallel lengths of wire; although the two ringing spikes are still present, their amplitude and duration are both much less severe. Figure 91, similar to Figure 89, indicates the potential severity of ringing and oscillations which can occur without careful attention to proper encapsulation and board design. In the two lower right panels of this figure, oscillations of increasing amplitude are apparent on the ground of the leaded flat pack, which occurred at a clock frequency of 1.25 GHz. Such oscillations are highly dependent upon board structure, encapsulant design, on system clock rate and on the harmonic content of the clock signal; in severe cases, the entire AC ground plane structure can exhibit an uncontrolled oscillation which completely defeats system operation.

These preliminary measurements of operational ECL and Gallium Arsenide components at frequencies above 1 GHz provide strong circumstantial evidence that leaded flat packs exhibit parasitic reactances too great to allow their use at extremely high frequencies; appropriate leadless chip carriers with very low parasitic reactances will be necessary. Second, the evidence is compelling that at these frequencies the design of the components, encapsulation, interconnect strategy, and circuit board operational parameters must be performed synergistically. We

believe that the research undertaken in this project for sub-nanosecond ECL is moving in essentially the correct direction for 250 psec risetime Gallium Arsenide components; however, the higher harmonic content of the Gallium Arsenide components will require a redoubling of these efforts to assure optimum system performance.

DIFFICULTY OF ACHIEVING GOOD QUALITY AC GROUNDS IN MULTI-CHIP DIGITAL GaAs/ECL SYSTEMS AT HIGH CLOCK RATES

(Flat Pack/LCCC Encapsulation; Negatively Shifted GaAs Supply Voltages; Wire Wrap Connections)

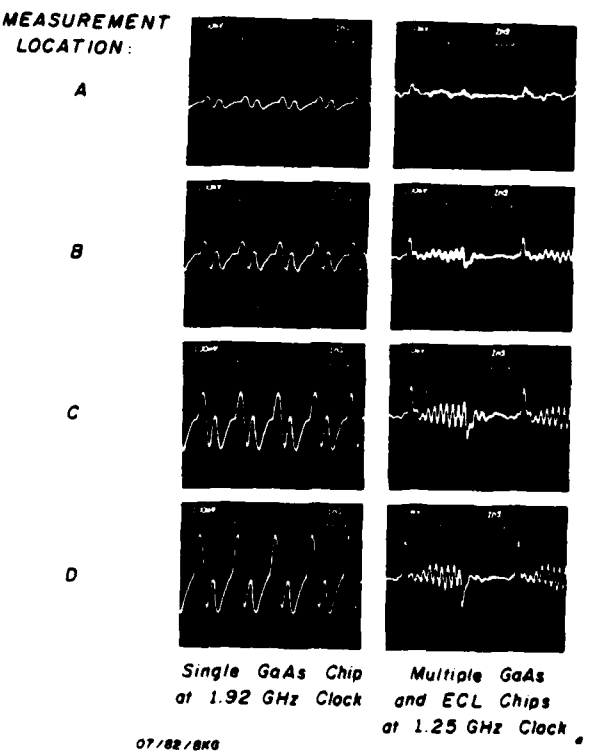


FIGURE 91

SECTION VIII

IMPROVEMENTS IN CAD/CAM SOFTWARE

Software to Support Graphical Design on an Intelligent Terminal

The goal of all Computer Aided Design tools is a decrease in the difficulty of achieving large, complex designs; manual pencil-and-ruler approaches which are feasible for small designs are rapidly becoming impractical for larger systems. Using digital computer design as an example, it is now increasingly necessary to automate the design rule verification process, to verify system timing, and to simulate all aspects of circuit function prior to prototype processor fabrication. Further, documentation which can be performed manually for small designs will have to be much more complete for larger projects. The tracing of a signal through a single page design is often difficult. When the design extends over ten or one hundred D-size print pages, the designer requires a legend on each page listing all networks entering and leaving that page, and extensive cross reference lists.

The incorporation into the CAD capability of several levels of abstraction, i.e., the ability to group transistors into gates, gates into functional blocks, blocks onto boards, and so on, is also important in a large, complex design. Several levels of abstraction are also necessary because attempts to design on a single level are too detailed for some purposes and too general

for others. In addition, a large processor frequently contains a considerable amount of repetition, particularly in the memory unit. The tedious redrawing of each memory element and its connection to other memory components merely stresses the patience of the designer. What is required in such a situation is the ability to build up one memory element in detail from fundamental components, a symbolic method of representing an N by M matrix of these elements, and the tools to allow the computer to generate all the internal connections between them.

The circuit information required to execute design rule checks, timing verification, and other automated CAD functions could be entered using a Hardware Description Language (H.D.L.). Reliance upon an H.D.L. requires either that each designer learn the language, or that one individual be assigned to a translation task. In either case, large designs would in many instances be hand-drawn first, and labeled carefully to avoid using the same name for different entries. Entry of descriptions into the data base could present a tedious typing task, and return communication with the user would also proceed slowly. For example, the computer might print: "Illegal connection, Component Number 125 pin A12 to Component Number 146 pin C6". The designer might be compelled to review all pages of the design to locate component 125 and component 146, recognize that the desired connection was to CG, not to C6, and then type into the computer:

"Disconnect 125.A12 - 146.C6"

"Connect 125.A12 - 146.CG"

Note that in this process the designer must refer to a "drawing" to ascertain the relationship between components 125 and 146, and then translate the correction into alphanumeric form, because the hardware description language processes only alphanumeric representations, not graphical constructs.

To speed the entry of large designs into the computer and to allow pictorial communication with the designer, we purchased an "intelligent" high spatial resolution color raster graphics terminal. Our intent was to provide an electronic drafting board, which would support both the graphical and the alphanumeric requirements simultaneously. While the designer "draws" the circuit diagram, the computer hosting or embedded in the terminal constructs a file with the same information that it would receive from a manual entry of H.D.L. information, thereby saving both translation time and entry time.

Mastery of this electronic drawing board is a "learn as you go" process. The novice is given simple directions, or prompts, as they are needed, from the computer. However, the user soon becomes "experienced" and can dispense with the instructions, which in turn greatly enhances the speed of communication with the computer. As an example of this interaction, in a variation on the example presented above, the computer prints "illegal connection" and blinks the wire path between Component 125 pin A12 and Component 146 pin C6. The designer immediately recognizes that the desired connection should have been to pin CG, not

to pin C6, and types "disconnect", then points the light pen at the blinking wire. The wire disappears. The designer types "connect", points the light pen at pin A12 and then at pin CG; the correct graphical connection is performed, and an alphanumeric representation thereof is added to the growing data base which represents the design.

USE OF HIGH-RESOLUTION GRAPHICS TERMINAL AND COMPUTER-AIDED DESIGN IN DEVELOPMENT OF ECL-BASED DIGITAL PROCESSOR

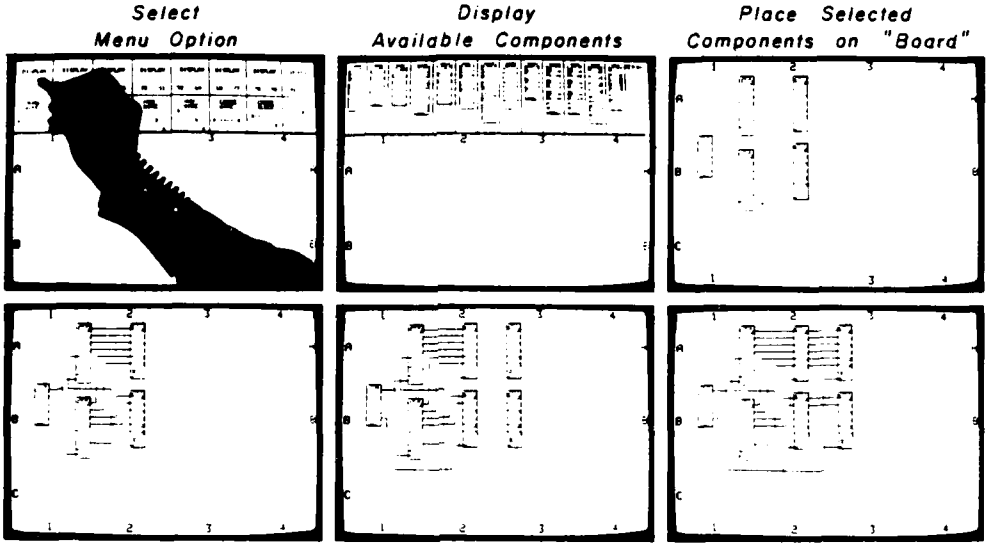
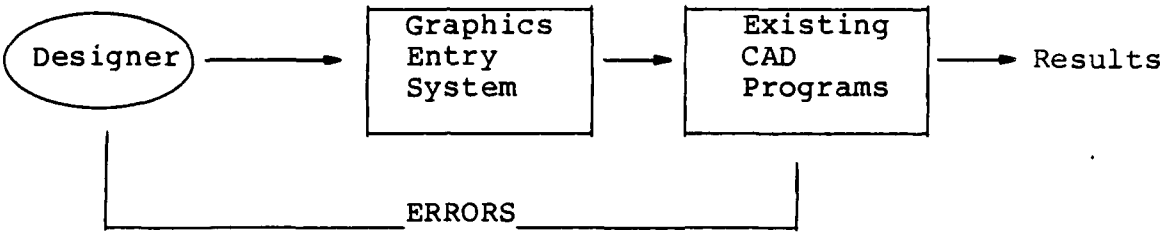


FIGURE 92

The ideal graphic entry system has proven to be an elusive concept, and may be different for each individual. A reasonable compromise system is under development at Mayo Foundation for use in our research environment. Input is performed via light pen, joystick, and tablet to control cursor movements, with a minimal amount of typewriter keyboard entry as needed. As depicted in Figure 92, the first step in a new design is the selection of component types which will be required, and their identification in or addition to the design data base. In general at least one new component must be added to the data base for each new system design undertaken, particularly as new components are designed and as new logic families, i.e., Gallium Arsenide, become available. The design is then built up by adding components and interconnects on the electronic drafting board.

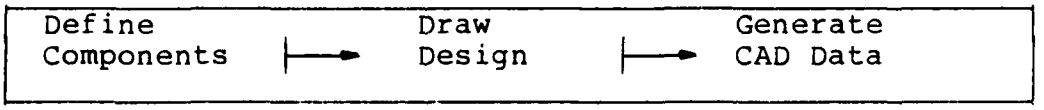
An important element of this method of performing a design is the mechanization and extent of design rule checking. There is a philosophical conflict between the performance of design rule checks while the engineer is laying out a new system, and the provision of instant response to the user. The more rule checking which is performed on-line, the slower becomes the terminal response. Presently no design rule checks are performed by Mayo's graphical entry system, in part because the time-shared mainframe host computer presently used for this task already exhibits fairly long response times (this problem will soon be

partially alleviated). Thus the graphics entry capability is a "front end" for the existing batch-oriented CAD programs, which in turn perform all design rule checks.

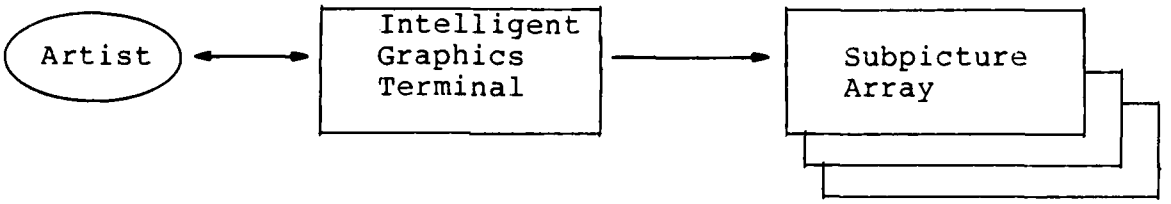


The graphics entry system has three major divisions. First, the "components" to be used in a design(s) must be defined in terms meaningful to the computer. Second, the designer "draws" a processor using these components, and connects them with lines representing wires or busses. Finally, data abstracted into alphanumeric form during the "drawing" process is correctly formatted for the existing batch-oriented CAD programs and downloaded to them.

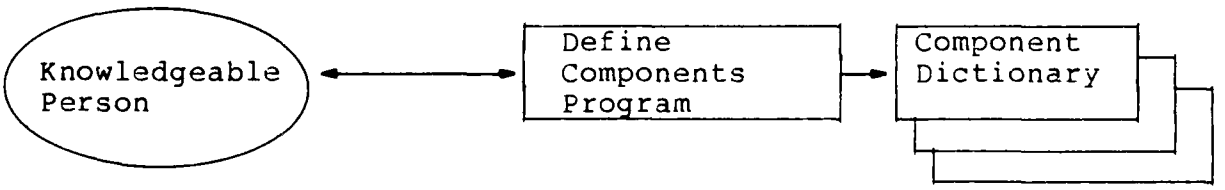
Graphics Entry System



The definition of a component for the design data base consists of two sections: a "picture" to be displayed to the designer, and the logical (alphanumeric) information to be used by the batch-oriented portion of the CAD system. The pictorial representations of the components are stored in a "subpicture array". Each subpicture is stored in a compact, encoded form, and must be interpreted by the intelligent graphics terminal, expanded, and redrawn by special hardware in the terminal. The initial entry of these subpictures and their storage into the array is performed locally on the Intelligent Graphics terminal.



A specialized software subroutine is then executed which generates entries in the "component dictionary", a file containing the logical information describing each component. Included in the logical information is a cross reference number which allows the graphics software to identify and retrieve the correct subpicture representation for each component.



The design engineer can then execute the program which assists in the generation or "drawing" of a new processor. A considerable effort was expended to assure that the design program would be "user-friendly". Since the complete graphics design capability will be judged primarily upon the ease with which it can be used by a hardware engineer, communication with the design program may be established in a number of ways. For example, the user selects each appropriate program function by typing single-letter commands; however, to refer to a location in the image before him, the user moves the screen cursor, either with joystick, light pen, key pad, or tablet and pen, and presses a special function key. At times a multi-character name is typed in and added to the image, to reference a component or an electrical network. Program functions available to the user include: the addition or deletion of a component, installation or removal of connections, addition of comments to the screen, and the regeneration of the design to create a "clean" picture on the screen. After the commands have been memorized, the user can turn off the tutorial instructions and suppress all prompts.

AD-A126 156 LEADLESS CHIP CARRIER PACKAGING AND CAD/CAM (COMPUTER-AIDED DESIGN/COMPUT..(U) MAYO CLINIC ROCHESTER MN SPECIAL PURPOSE PROCESSOR DEVELOPMEN.. 3/3

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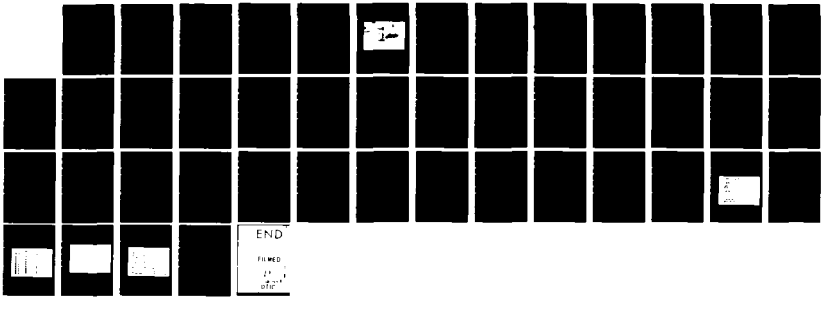
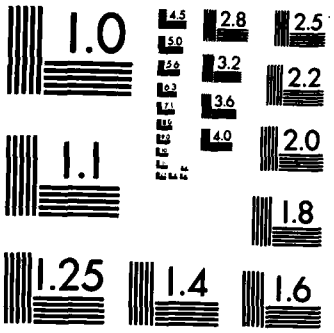
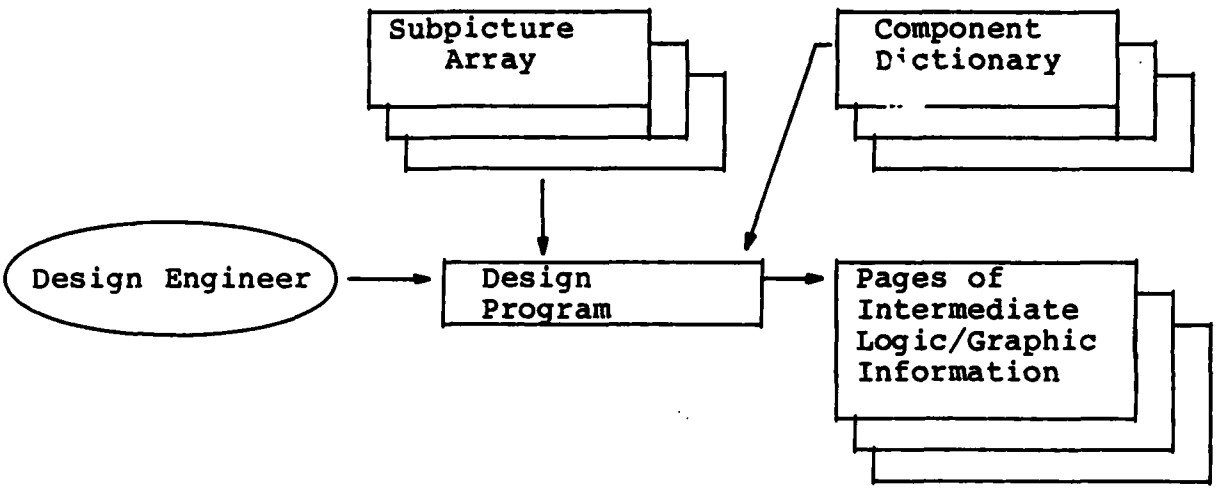
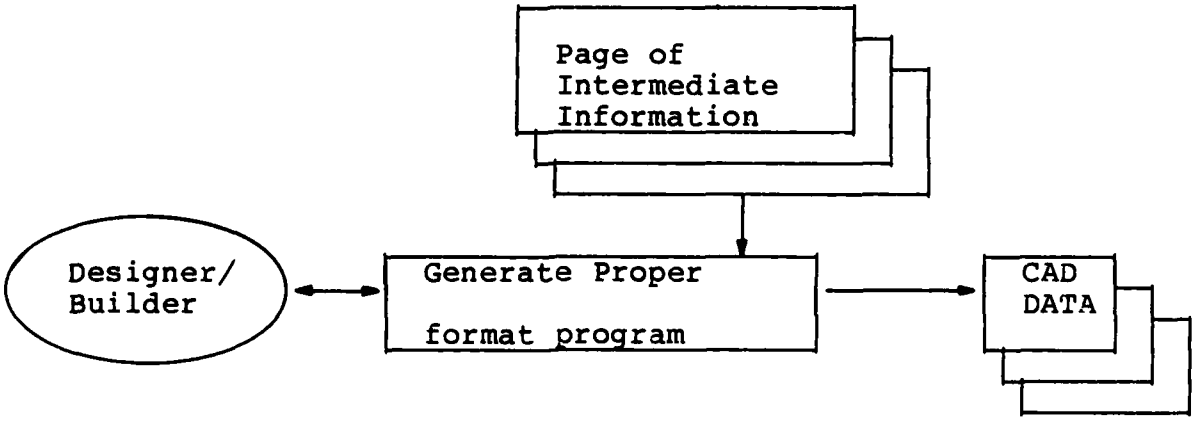






Alphanumeric information abstracted from the graphical design can be reformatted into the data input structure required by the existing offline CAD programs. Presently, either the designer or the fabricator of the new system must enter the type of physical package which will be employed for each component when the system is fabricated, but this process will soon be simplified and automated.



In this first developmental version of the graphics interface, there remain many instances of tedious question-answer interaction between the terminal and the user, which could be considerably simplified through graphical interaction. More importantly, the present graphics input system is being expanded to include the use of macro definitions, thereby to support the macro capability already extant in the batch-oriented portion of the Mayo CAD package. As will be discussed later, logical and physical macros will be especially important in the design of gate and macrocell arrays. Although there is a quantum difference between the design of a gate at the transistor level, and the interconnection of hundreds or thousands of these different "gates", nonetheless both of these design tasks should be performed on the same CAD system to allow the maximum interaction between them. For example, if an impasse is reached during an attempt to route connections around or between gates, a solution might be achieved by descending one level of abstraction and redefining the layout of a few "gates" so that they have a higher internal functionality and require fewer interconnects to be routed around them. With the recent addition of a UNIX-like operating system to our intelligent graphics terminal, it is planned to perform more computing locally, thereby decreasing response time through the exploitation of the "dedicated processor" in the terminal. Faster response time can permit more design rule verification at run time without frustrating the designer.

System-Level Computer Aided Design and Manufacturing (CAD/M) Package

Development of the Mayo Subnanosecond ECL CAD/M package has continued during the past year. The main goals of this expansion effort are intended to achieve improved capabilities in the design verification, fabrication and checkout phases, and to make it more flexible, automated, and easier to use. The fundamental skeletal structure of the package has remained unchanged since this version was designed 2½ years ago.

As a brief review, the major steps taken during the CADing of a design, and described one year ago, are:

1) generation of a skeletal data base that defines the physical and electrical characteristics of the wirewrap board;
2) generation of a component dictionary;
3) definition of pin nets that are specific to the circuit under design;
4) assignment of components used in the circuit under design to the logic board data base;
5) connection of pin nets within the logic board data base;
6) verification of the physical design (i.e., application of design rules);
7) termination and application of ECL transmission protocols;

8) generation of documentation;

9) generation of numerical control tapes to drive fabrication equipment;

10) interaction with the design data base for checkout and testing assistance and for the generation of engineering changes (see Figure 93).

The following material will summarize enhancements and minor changes made to the capabilities listed above, report new features added to the package, discuss current work, and finally, will present ideas for the future.

USE OF A COMPUTER TERMINAL TO PROBE THE CAD DESIGN DATA BASE DURING BENCH CHECKOUT OF A NEW HIGH-SPEED ECL PROCESSOR. BLUEPRINTS NEED NOT BE EMPLOYED.

FIGURE 93

Enhancements

Several capabilities already in place a year ago were further modified as a result of actual use and experience; these changes will be summarized first.

The logic string termination routines were provided with an operator-interactive capability to permit the designer to restrict the use of non-standard terminator pack (SIP) assignment locations. The goal of this procedure is the termination of all signal strings according to pre-established termination protocols while minimizing "bunching-up" of terminator packs and the need for special board preparation of the terminator pack installation locations.

The paper tape punch/verification programs were provided with an interactive capability to allow convenient "blocking" of portions of the punched output, a requisite since the output for a single board requires more than one tape reel. In addition, the grid size of the board was converted into a variable that can be ascertained from the data base by the punch routine, and then used in a determination of wire wrap step size.

New wire wrap methods were determined on the basis of the results of several design and fabrication projects. The wirelist program now partitions wires into three groups: data signals, clocks, and I/O (i.e., wires to and from cable connector sockets). Within these groups, the wires are sorted by length,

partitioned into two wrapping levels, and specified in terms of wire lengths that are available in pre-cut sizes.

The documentation package was enhanced through the provision of several new modules: 1) physical pin net-listing; 2) I/O connector documentation; 3) termination requestor pin listing; 4) a net-length analysis subroutine.

The data base interface routine now prints out component and interconnect statistics at the termination of the job; these results are useful for monitoring activity, comparing designs, and for determining possible design optimizations. In addition, generalized "open" and "close" routines are now used by every program module. As a result, numerous "universal" tasks are now performed in a concise and consistent fashion.

The attribute field in the data base records is now packed into two data words regardless of the type of attribute, in turn permitting a larger total number of attributes. Packing and unpacking are handled by the data base interface, making this operation transparent to the calling programs. Several new attributes have been adopted for graphical descriptions of components and board sockets. The structure of the status communication file was defined more rigorously; several new parameters are now being stored in this file.

Non-standard or "custom" components, e.g., DIP switches, momentary switches, LED indicators, voltage controlled oscillators, etc., have always presented problems for the CAD. As a result, a new mechanism to process such components has been adopted. The individual components which comprise the custom parts are mounted on a DIP header and added to the component library, thereby reducing problems associated with component auto placement and board preparation.

The method of generating a new board design was also modified. Following this modification, board sockets are described and entered into the component dictionary, thereby allowing socket pins to be assigned multiple attributes (previously, each pin could only have one attribute). The process of defining a board by placing various socket types on the surface of a blank board is very similar to the assignment of components to the board. Socket labeling is now also completely flexible, as the labels do not depend on row or column configurations.

New Features and Current Work

As experience is gained and the CAD is used in additional designs, new features have been identified and implemented fully,

or are in an experimental stage. Some of these features are specific tasks specified in the program schedule, while others were determined during development to be necessary.

Graphics Terminal Interface

A subroutine which can be called by a FORTRAN routine was created to provide a convenient interface to the Chromatics CGC 7900 graphics terminal described earlier. This new routine converts input commands such as "draw rectangle", "set color", "read cursor position" etc., into character strings interpretable by the CGC 7900, and buffers them for output. This routine is used by a manual component placement module and by a board graphics module.

Plotter Interface

Since the arrival of our Calcomp Plotter three months ago, two experimental software modules have been prepared, both of which in turn call routines supplied by Calcomp Corporation for the CYBER computer. One of these new programs draws the board configuration, including socket outlines, pins, and socket names; the other routine draws the geometry and pin labels for all of the components defined in the dictionary. These plots are useful in the maintenance of a component/board notebook for documentation purposes.

Alphanumeric Terminal Interface

An interface subroutine between elements of the CAD package and the alphanumeric screen (in our case, the Televideo TVI-920C) was written to provide a method of utilizing some of the special functions available in the terminal hardware, such as erasure of the screen, erasure of a specified line, placement of the cursor at a desired position on the screen, and so on. This routine is now only used by a few special menu programs, but will eventually be used by all subprograms.

Analog Simulation

During February 1981, we installed Version II of the SPICE circuit simulator on Mayo's CDC CYBER computer. The SPICE package stands alone at present, i.e., is not coupled with the remainder of the CAD package. Future plans exist to incorporate the analog simulation capability of SPICE into the CAD as hierarchy and analog models are further enhanced.

Logical Database

It became evident that the ability to perform certain manipulations on the logical design prior to physical CADing would be a desirable and powerful feature. Previously, the vast majority of the design rule checks were not applied until components had been assigned to locations on a logic board and the nets wer connected. Since automatic component assignment has been i le- mented, and additional design verification stages will be d - loped which will be executed prior to physical CADing, it i clearly an advantage to detect as many design rule errors as early as possible at the logical design stage. The concept of generating a database from the logical description, independent of physical parameters, has been partially implemented.

The logical database is identical to the physical database except that data fields in the records related to physical logic boards are not used. However, because both databases are of the same structure, all of the established interface and data manipulation routines can be used directly. This logical database will be used for logical design/rule/verification and timing analysis, and for logic simulation.

The logical design still retains several physical dependancies; for example, the design must still be expressed in terms of physical components. Current designs use integrated circuit packages as the basic building blocks. Presently, when

hierarchical macros are constructed, the smallest irreducible components are still integrated circuit packages. Thus, the logical design is closely coupled to existing physical components. The logical database does ignore component placement, net-connection configurations, ECL terminations, and transmission protocol. Steps will be undertaken in the near future to remove these last remaining physical design dependencies as well.

CAD Supervisor Routine

Because the number of software modules in the CAD package has become so large, and because of the difficulty of executing these modules in the proper sequences during a design run, a supervisory program, or "supervisor", has been written to provide an organization to the separate modules and options. This organization provides the following benefits:

1. The user always logs into one program.
2. Options are displayed in menu form.
3. The user need not be concerned at all about file names; the various files now appear to reside within a single unified database.
4. Coexisting multiple designs are now possible because the corresponding files are partitioned by a unique design name key.
5. Design activity can now be monitored and archived.

6. Several modules performing different stages of a design task appear to be only a single entity to the user.
7. New modules, options, and utilities are easily incorporated into the supervisor by modifying menus and adding new procedures (i.e., a job control language file).

The supervisor consists of three programs which converse among themselves through a communication file. These routines are activated by means of a procedure on the Control Data Corporation CYBER 720 which contains a loop. The looped procedure and communication file are necessary on the CYBER because of the inability on this computer to execute job control language statements directly from a FORTRAN program. Job control is performed from the supervisor by creating a procedure file and pausing the program to initiate the execution of the procedure file.

The first supervisory program requests the user to supply a design file key, i.e., a five character string which is then used to create names for all files associated with the design. The communication file associated with each specific design is then copied into the "working" communication file. The second program requests the user to identify the type of terminal he is using at that moment. Currently, the Televideo TVI 920C alphanumeric and the Chromatics CGC7900 graphics terminals are supported. A flag is set in the working communication file specifying the terminal type.

The third program, the main supervisor, reads the first record of the working communication file to obtain the type of terminal in use, and the previous step executed. The main menu provides the following options on the display screen:

A. Run job;

B. Route printout from last step;

C. Define design;

D. Review design steps;

E. Examine design status;

F. Initialize design files;

G. Store design files;

H. Retrieve design files;

I. File edit;

J. Modify component dictionary;

K. Exit.

These options will be briefly described below.

A. Run Job executes a CAD step. The currently available options are:

1. Schematic design;
2. Extract files from a schematic design;
3. Logic simulation (currently under development);
4. Timing verification (currently under development);
5. Generate a new board design and layout;
6. Initial component placement;

7. Component placement optimization;
8. Assign components to a logic board;
9. Connect signal nets on the logic board;
10. Board design verification;
11. Transmission line logic termination;
12. Transmission line logic interconnect;
13. Board design documentation;
14. Wire listing;
15. Punch a paper tape;
16. Verify paper tape;
17. Board design debug/trace;
18. Board graphics display;
19. Board plotting;
20. Engineering change.

B. Route Printout routes the print file generated in the previously executed step to the line printer.

C. Define Design is executed when the designer initiates the layout of a new processor. The following parameters must be supplied by the user:

1. a title or name for the design;
2. special comments;
3. the type of circuit board to be employed;
4. a definition data file for the logic board characteristics;

5. the logic component family to be employed (e.g., F100K ECL);

6. a definition data file for the component family.

Following the input of these specifications, the design files are initialized.

D. Review Design Steps allows the user to view all of the design stages that have been performed to the present.

E. Examine Design Status displays the current status or progression level of the design.

F. Initialize Design Files allows the user to reinitialize specific files without having to redefine the entire design.

G. Store Design Files in its present embodiment condenses all design files down into one multi-section file (i.e., a "multi-file file"). Later, this step will be used for the creation of a tape archive of a particular design.

H. Retrieve Design Files currently re-expands the "multi-file file" into its individual component files. Also, in the future this procedur will be used in the retrieval of a design which has been archived on magnetic tape.

I. File Edit allows the engineer to employ the system text editor to modify or examine the following files: 1) board definition

input; 2) component assignment input; 3) printout from the previous job step; 4) printout from the current CAD session; and 5) printout from the design achieve.

J. Modify Component Dictionary allows the user to review and/or modify the contents of the component dictionary. The two options available are: Print Dictionary or Modify Dictionary.

K. Exit exits from the CAD supervisor.

Automatic Component Placement and Placement Improvement

Automatic initial component placement and placement improvement capabilities have been incorporated into the CAD system, have been employed in several recent fabrication projects, and appear to work very well. For wire-wrap technology, which can be considered to employ a point-to-point interconnection strategy with no concern for crossovers, a natural criterion to use in placement and optimization is a minimization of the total wire length on the logic board. This is the "classic" criterion, and has been used in many CAD systems.

The development of the auto-placement capability was initiated by coding an experimental set of software routines. The initial placement algorithm was the so-called "pair-linking" constructive placement, which operates in the following fashion:

1. The pair of components (modules) exhibiting the highest connectivity is placed in the center of the board.

2. Individual modules that have the highest connectivity to the two modules placed on the board in the first step are positioned as close to the original cluster as possible.

The cluster then "grows" until all of the components are placed. When all of the components are placed, an improvement algorithm is then applied. The method used in this experimental system was the "force-directed interchange" method. Modules are repositioned according to the "forces" (i.e., the number and direction of connections) that are exerted upon them. These algorithms were actually tested against an ECL system design and demonstrated a 24% greater total wire length than that achieved through laborious manual placement by the designer. Such a degradation may be acceptable because a considerable saving of the designer's time is achieved. However, if the performance of the system under design is adversely affected by the automatic methods, then clearly the benefits of the auto placement are questionable. A direct comparison of the system performance of the hand-placed and the auto-placed designs was not performed.

The auto placement algorithm finally incorporated into the CAD system is a pairwise exchange algorithm with random or manual initial placement. The primary reason for the adoption of this approach was the simplicity of the algorithm. This pairwise exchange algorithm easily allowed the incorporation into its

structure of the various parameters which must be accomodated in the logic boards presently in use or envisioned. These special considerations include: 1) the requirement to employ multiple component sizes and shapes; 2) the use of numerous board socket types; 3) a variety of board configurations; 4) the occasional assignment of more than one small component to a given board socket; 5) the required provision for the prior manual assignment of special component types into designated locations; 6) the ability to define specific signal nets (e.g., clock strings) to be more "important" than others.

The initial placement algorithm requires the following items of input information: 1) a list of modules employed in the design; 2) a logical connectivity list between the individual modules; and 3) a board socket list. The module list contains the module name and its "part type" (transferred from the schematic), and the type of mounting socket required by the module (this information is obtained from the component dictionary). Connectivity information is derived from the net list, which is in turn obtained from the schematic. The board socket list, which is obtained from the skeletal data base created at the time of board generation, contains the socket name and socket type. Random initial component placement can be executed with no operator intervention, since the software simply assigns modules to random sockets of a suitable type. The outputs from this program are two "card image" files. The first of

these files is specifically formatted for use by the assignment program, which assigns the modules retrieved from the database to specific locations on the board. The other file serves as input to the placement optimization software. The manual initial placement program is designed to operate interactively with the user through the intelligent graphics terminal described earlier. This program employs the same input information as described for the random placement algorithm, as well as additional graphical data that resides in the skeletal database. A cartoon of the logic board is presented on the screen to the designer, who then places the components using the joystick cursor. As with the random placement program, two files are produced.

The optional placement "optimizer" requires as its input a file from one of the initial placement programs, as well as board information from the database. Its operation is very simple conceptually; all possible pairs of modules are examined, and the relative positions of both members of the pair are interchanged. If the total board wire-length is improved by the exchange, the two modules are left in their exchanged positions. After all modules are compared in this manner, a second iteration is performed. Iterations are continued until either a specified maximum number of exchanges have been performed or the total wire-length can no longer be improved. The resultant placement is "quasi-optimal"; the "quality" of the final placement is heavily dependent upon the quality of the initial placement. However, in the experimental runs tested to the present, the results from

different initial placements appear to generate quite similar total wire lengths. As an example, for a test design, discussed earlier (the pipelined convolver/correlator), random initial placements with total wire lengths of 935 to 1358 arbitrary units yielded optimized final results of 852 to 899 arbitrary units respectively with force-directed methods, and 851 to 884 arbitrary units when the pairwise exchange algorithm was employed.

The placement optimizer program itself can account properly for modules in pre-established locations, multiple modules in a single socket, and nets which are considered of more importance than other nets (these special nets are said to be "weighted"); however, these options are not currently supported by the initial placement algorithms. The optimizer creates a revised file to be used by the component assignment program, which in turn updates the database.

Hierarchy

Hierarchy plays a vital role in Computer Aided Design by allowing a computer architect to work in a top-down, structured-design environment, and also in a bottom-up modeling environment. The entire CAD package must in general depend heavily on hierarchical concepts from the viewpoint of the logical design (i.e., schematic drawing, simulation and verification), and also

from the view of the physical realization of the design (i.e., physical packaging, organization, partitioning, placement and device technology).

A very simple single-level hierarchy capability was fully integrated into the CAD package during the past year. A system design was undertaken in which several copies of one structure were required, each of which was completely independent (since the individual copies communicated with one another through cable connectors, this independence was more apparent than actual). A net-specification macro library program was prepared which stores design information to be used on the next higher level, i.e., at the "macro call" level. The required input data for the macro-library program is a macro name, as well as a list of "input lines". For the system mentioned earlier which was designed in this manner, the input lines were the net specifications (net-name, page, component-label, pin-label). Whenever the macro-call parameters (in this case, one character string) are desired, a special symbol is used (a "#"). The "input lines" are stored in the library according to the macro name which appears in the library directory. Later, when the macro is retrieved (called) from the library, the lines are read from the library, with the macro call parameter inserted where specified.

In the test design, the macro net specifications were stored, using the Macro Definition program, and were retrieved by

the Net Specification program. This was the only program to be given macro call capabilities. For example, suppose the following were to be stored in the macro library:

```
NODE
#NET1 01A1 #01 A1
#NET1 01B1 #02 B3
```

Then the following macro calls appearing in the net specification input:

```
. NODE 1
. NODE 2
```

would produce the following net specifications:

```
1NET1 01A1 101 A1
1NET1 01B1 102 B3
2NET1 01A1 201 A1
2NET1 01B1 201 B3
```

This very simple macro structure served as the initial test vehicle for these developments, but is very limited in its scope. Only the net specifications are supported, and then only these nets that are completely internal to the "macro" can be handled properly.

A more general form of hierarchy has now been defined, and a test program has been written and executed successfully; however, this newer algorithm has not yet been integrated into the CAD

package. A brief description of this new approach will be presented.

Any design can be completely described by the following information: 1) Name and design level; 2) Connections that are accessible from the external environment; 3) A list of logical blocks that are employed; and 4) A list of connections between these blocks. If this information is stored in a library, and if a suitable "expansion" algorithm exists, then the blocks that are referred to in Item 3 above can be "expanded" to reveal their internal structure, and can also be incorporated into the structure within which they were referenced.

A top-down design capability can then be supported by allowing the design to be subdivided into interconnected functional blocks, which are referred to as "macro-blocks". These in turn can be independently designed in terms of interconnected "functional" blocks. At the lowest level, a macro block is defined in terms of special "functional" blocks, for example, ECL 100K integrated circuits, gate-array macros, logic-level simulation blocks, or analog-level simulation blocks. A bottom-up design capability can also be supported by allowing blocks to be built up from special "primitives," and further incorporated into higher level blocks.

The algorithm for expanding a design from the most to the least complex levels, i.e., "top-down", assumes that the top-level design resides in the macro-library as well as the logical blocks at all other levels. A macro block consists of the following:

```
NAME:  name, level
EXTERNALS:  name, netname
            *
            *
BLOCKS:  blockname, blocktype
            *
            *
NETS:  netname, blockname, blockpin
            *
            *
```

The following steps represent an outline for the expansion of an input macro by one level. The output itself looks exactly like a macro specification, and can be further expanded by the same procedure in an iterative manner. Several semantic terms used below must be defined first: "Input" refers to the macro being expanded, while "output" refers to the expanded macro.

1. The input name and level are used as the output name and level.

2. The input externals, which consist of an external name and a netname associated with the external, are used as the output externals.

3. For each block, its blocktype definition is retrieved from the library. The blocks used in the definition then become the output blocktypes. The output blocknames are obtained by concatenating the name that appears in the definition with the name used in the input.

4. For block interconnects, the netname used in the input is carried down into the net appearing in the library definition of the specified blockname-blockpin.

5. For nets completely internal to the block being expanded, a netname consisting of the internal netname, concatenated with the blockname, is used.

An example is useful in explaining the procedure. Suppose the following library is defined:

```
Name:  MACRO1
Externals:  INP NET1
            OUT NET3
Blocks:  BLK1/BLK1  MACRO4
         BLK2/BLK1  MACRO5
Nets:  NET1 BLK1/BLK1  INP
       NET2 BLK1/BLK1  OUT
       NET2 BLK2/BLK1  INP
       NET3 BLK2/BLK1  OUT
```

MACRO1 is now defined in terms of MACRO4 and MACRO6. Since MACRO2 and MACRO3 were very simple (i.e., they contained no internal nets), no new nets were created in the expansion.

This scheme guarantees unique netnames and blocknames, provided that each block in the library has been defined correctly. In addition, an examination of the result of an expansion reveals that a blockname or netname completely describes its origin. The procedure can be repeated a given number of times; repetition of the procedure can also continue until all blocks in the input are at a specified level or can be expanded no further.

The main drawback to this method for the current CAD package is the accompanying growth in the length of the netnames and blocknames. However, this limitation can be accommodated by means of a separate file containing the sorted names, with retention of the record number of the name in the current database.

Logic Simulation

Logic simulation serves as an important design validation step inserted between the schematic design and the physical realization of the system, i.e., fabrication. A small test simulator was coded, and demonstrated to be operational on several small designs consisting of a purely combinational circuit, a

sequential circuit, and a circuit utilizing a general delay element and feedback (to test the effects of oscillations). In the test simulator, three logic states were supported: logic 0, logic 1, and undefined. It may be useful to support additional states in the future as more comprehensive descriptions of the device technologies become available.

Of primary importance to the simulator is the representation of the circuit within the data structure; the data structure was established using data statements in the simulator itself. At present, the simulator is not supported by the comprehensive CAD package; integration of the simulator into the CAD package will necessitate the construction of the data structure from the database, and the support of logic functionality in the component dictionary. The devices currently modeled are:

1) 2 input AND; 2) 2 input OR; 3) NOT; 4) D-type flip-flop; and 5) Delay Element.

If these generic types can be proven first, other devices more relevant to the ECL design environment can be derived directly, or assembled from the above-described generic types.

The initial version of the data structure consists of a "node table" that describes:

1) the type of node (logic element);

2) a pointer to a data table;

3) the number of inputs;

4) the number of outputs; and

5) a data table that contains the following information for each input/output of a logic element:
   a) a pointer to the next pin in the signal net
   b) the current logic value;
6) also present is a structure to describe each input signal:
   a) a pointer to the location in the data table which receives the signal;
   b) the initial value; and
   c) a list of transition times.
7) A structure for identifying the output signals (i.e., which signals it is desired to examine), i.e., a list of pointers to the data table where output signals can be retrieved.

The initialization phase consists of the following steps:

1. initial input states are applied to the system inputs, and input events are scheduled;

2. if there are no scheduled events, outputs are generated and the program skips to the simulation phase;

3. logic functions are performed;

4. events are scheduled;

5. Go to step (2).

The following is the simulation procedure executed for each time point:

1) If there are no scheduled events, process all outputs and go to the next time point;
2) Perform logic functions;
3) Schedule events; and
4) Go to step (1).

The output processor in the test simulator generates traces on the Chromatics graphics terminal screen to emulate a hardware logic analyzer. In addition, a printout file is generated for later reference.

We have identified numerous possible enhancements to the simulator which will permit its integration into the CAD package, and which will improve its efficiency. The primary goal of these first experiments was a verification of the feasibility of the general approach to simulation. Several improvements already under development include:

1. the creation of a structure that facilitates the fanning-out of a signal to its destinations in one step;
2. provision for storage of each signal and the occurrance time of its last state change--this technique will be used in the identification of timing errors arising within sequential circuits;

3. creation of the data structure directly from the database;
4. the establishment of convenient representations for the specification of input signals;
5. the storage of all outputs in a file during simulation, which will allow the user to interact with the file through the graphics screen (i.e., to simulate the probing of a hardware circuit);
6. the development of faster and more flexible methods of performing the various logic functions.

Timing Verification

It is frequently both desirable and necessary in a high-speed logic design environment that timing verification/analysis be executable as a separate operation from logic simulation. An accurate logic simulator will detect timing errors arising from the application of the specified input signals; however, since it is usually not possible to apply all combinations of inputs, certain timing problems may still exist and not appear until the system is fabricated.

Two major types of timing verification schemes have been described. The first is a logic simulation using generalized states which represent time-dependent behavior. The second

method is based upon an analysis of path lengths in one form or another. Both methods may be used to detect the following types of errors:

1) set-up/hold time violations;
2) clock skewing effects; and
3) pulse width problems (i.e., slivers, runts, race conditions).

The data required to detect such errors are component-dependent parameters, including: set-up times, hold times, gate propagation delays, rising and falling edge durations, and gate inertia; and interconnect dependent parameters, i.e., layout geometry, propagation media and signal string loading.

The initial implementation of a timing verifier performs the following general tasks:

1) identification of primary clock inputs, and the phase relationship of clock signals;
2) identification and analysis of the clock distribution network;
3) partitioning of remaining design elements into sequential logic and combinational logic;
4) analysis of partitions, and their relationship to the clock distribution network; and
5) performance of path analyses.

At present our approach to timing verification is considered experimental. A first-attempt verification capability is being installed currently, to be applied to the logical designs prior to physical implementation. The interconnect nets at this stage in a design are "idealized", i.e., they are independent of actual physical parameters, for which reasonable approximations are presently included as estimated constants. It is intended that the verification will also be executed after the design has been committed to a physical layout but prior to fabrication. The ability to model interconnect nets accurately is already available.

Partitioning

One method of releasing the design process, at least in part, from the physical component configuration is through the direct exploitation of logical subunits of a single integrated circuit. For example, if a chip contains six D-type flip flops, the designer should be allowed to use the individual flip flops as building blocks, and to consider them as separate entities. When a physical implementation is finally derived from the logical design, these logical elements have to be mapped onto the integrated circuits, a process referred to as "partitioning." The partitioning process in general invokes graph-theoretic techniques, and is dependent upon the physical layout and connectivity of the elements in the design.

Gate/Macrocell Arrays

Initial conceptualization studies have been performed to assess the best methods of injecting gate/macrocell array technology directly into the existing CAD package. Gate/macrocell arrays are of special interest in a prototyping environment because they can provide quick turnaround design and fabrication of specialized components that are extremely useful in high-speed processor architectures.

The design process and physical layout in a gate/macrocell environment is similar to the board-component approach to system design presently supported by the Mayo CAD/M package. Predefined gate array macros are nearly equivalent conceptually to integrated circuits, and the gate array cell structure is conceptually similar to a logic board. It appears at present that the design database can directly support gate/macrocell arrays.

Several fundamental differences between logic boards and gate/macrocell arrays have been identified, and must be accommodated.

1) Macros are not necessarily a rectangular configuration of cells. Thus automatic placement must acquire the capability to manipulate shapes much more complex than rectangles.
2) Macro I/O contact pads may have multiple and/or variable locations at the edge of the macro, which in turn affects the net connection software.

3) Optimizations of each macro which generate tradeoffs between speed and power are psssible, and must be supported with appropriate software.

4) The interconnection of macros will necessitate the use of a specialized interconnect router which must solve the routing problem using only narrow routing channels.

5) The use of special I/O drivers on the periphery of the cell array structure will be a partially new feature in the Mayo CAD package. It may be feasible to handle these peripheral structures in a manner similar to the presently implemented receivers/drivers and off-board connectors.

Printed Circuit Boards

A multilayer printed circuit board package is currently being installed on our CYBER computer. This independent package, obtained from the NASA software distribution center, supports multilayer boards with completely unconstrained geometries. However, this package does not account for transmission line interconnects, making it necessary for us to tailor the signal routing algorithm to increase efficiency and orient its layout rules for that type of environment. Eventually, the printed circuit board package will be fully interfaced to the database and CAD supervisor as another application module, and will be presented to the designer as an option. The output of the package

is a BANNING artwork file that can be check-plotted on a Calcomp plotter or transmitted directly to a Gerber film plotter for the direct creation of board fabrication artwork.

Future Directions

The long term goal for this CAD/M development is the presentation to the designer of a useful set of tools in a structured design atmosphere, optimized for high-speed device and system technolgoies. Ideally, logical design and physical realization should be concerned only with the creative tasks of design conceptualization and specification, while the physical implementation should be performed by the CAD. The designer should be given a broad range of specification and simulation tools to provide immediate feedback concerning the operation and performance of the evolving design.

Several of the topics in the last section are currently being addressed and will continue during the coming year. Several new topics, conceptualized recently, will also have to be addressed:

1) enhanced capacity for high-speed interconnect modeling;
2) architectural level specification, modeling, and simulation;
3) hardware description language capabilities;
4) database unification;

5) improvements in the power of circuit level modeling/simulation tools;

6) inclusion of microcode/microsequencer simulations;

7) fault simulation/testing; and

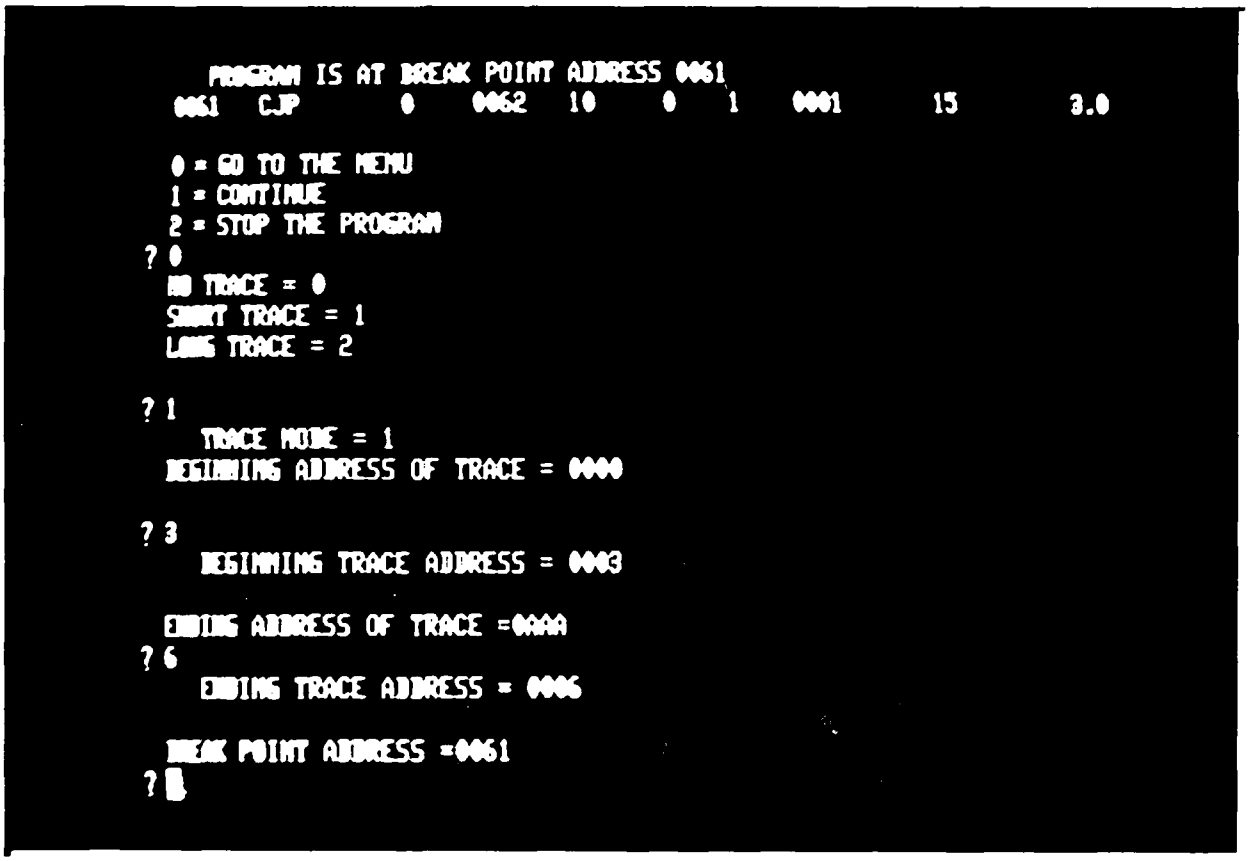
8) automated speed/power optimization capabilities for all arrays.

SECTION IX

MICROCODE DEVELOPMENT AIDS AND MICROSEQUENCER DESIGN

During the past three years, it has become apparent that, as large processor systems become more complex and more distributed, the control of these systems will become more difficult. It gradually became evident that the development software support aids for, and a useful description of, an efficient microprogram sequencer would be a valuable asset to our comprehensive CAD/CAM capability. Such microsequencers can serve as high-speed control engines of limited intelligence for use in the resource management of a variety of arithmetic processors. Therefore, in this research project we have developed a special software package, or "meta-assembler", which assists in the preparation of control programs for these microsequencers. The meta-assembler, also sometimes called a macro-assembler, is written in FORTRAN, has been installed on Mayo's CDC CYBER 170/720 computer, and is configured initially to support the instruction set of the commercially available AMD 2910 microprogram sequencer.

In addition, a preliminary software simulator has been developed to allow semi-automatic testing of microcode written for the AMD 2910 microsequencer. The AMD 2910 simulator program employs an interactive computer terminal to display a menu, as in Figure 94, from which the user may specify or modify any of a number of options; alternately, the simulation can continue to



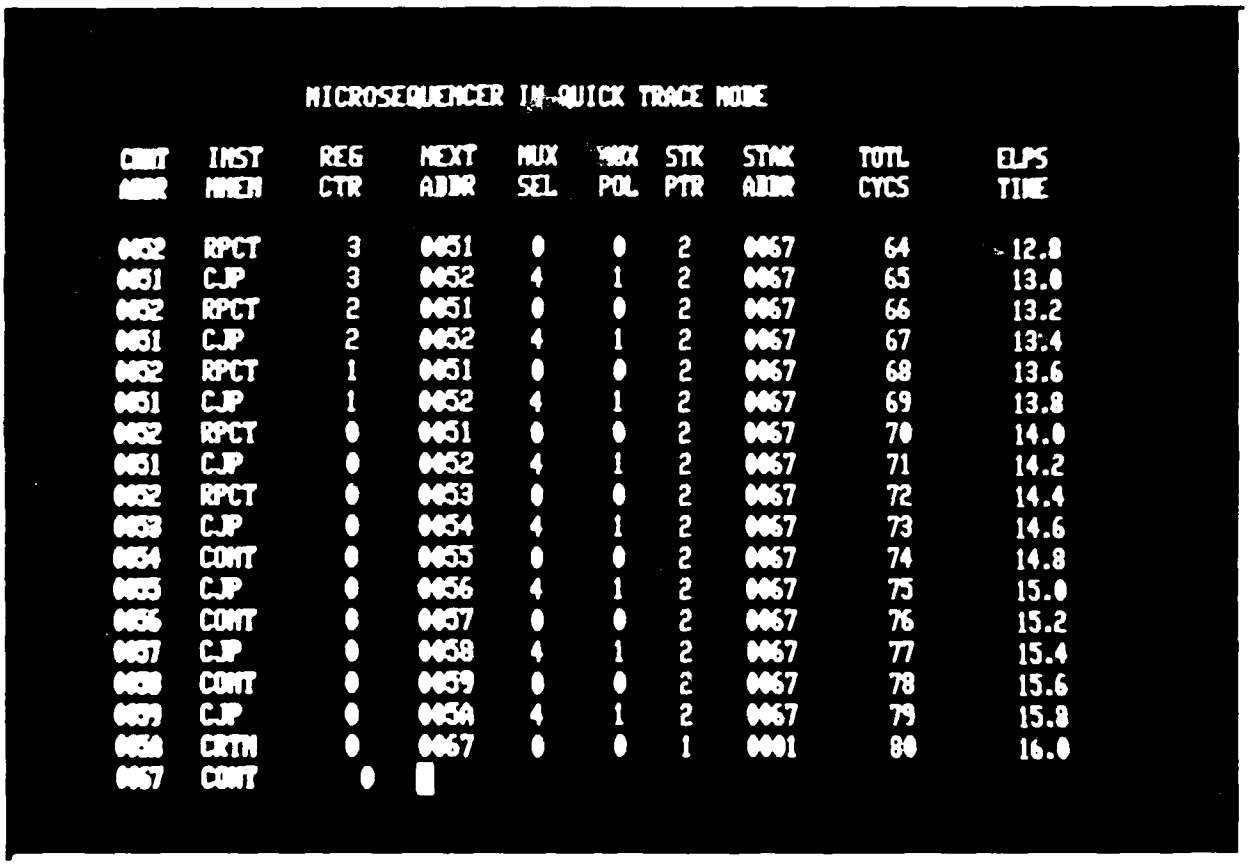
PROCEDURE MENU OF MICROCODE EXECUTION SIMULATOR DEVELOPED TO SUPPORT MICROPROGRAMMED CONTROLLERS.

FIGURE 94

the next breakpoint or to the end of the program, with the options remaining unchanged. The trace option can be invoked at any address in the program being simulated, and may be left in effect while one or any number of instructions are executed, or until the end of the program is reached. The starting and ending addresses of the trace may be changed whenever the simulation has stopped at a breakpoint.

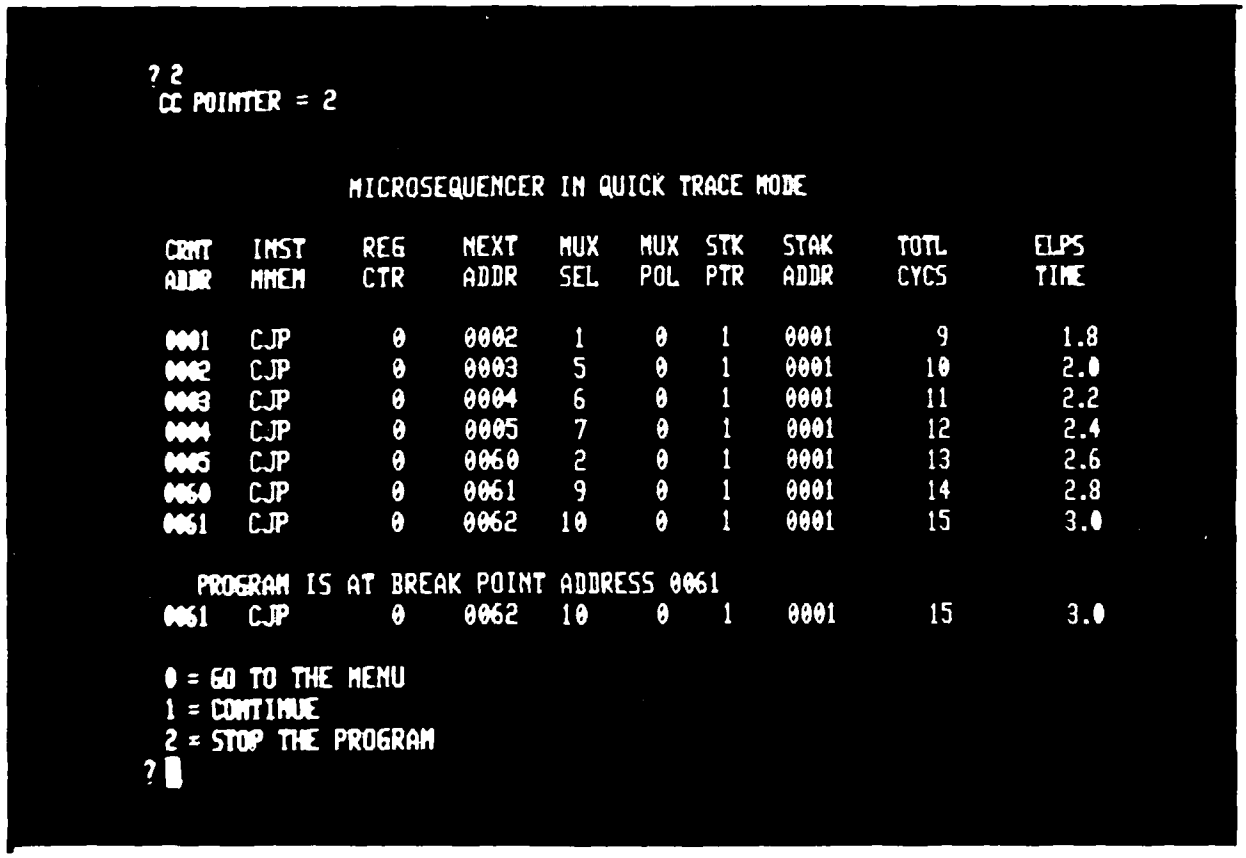
The short trace or "quick trace" mode is designed to be very dense, with only one line displayed on the video terminal for each instruction. As shown in Figure 95, the address of the current instruction, the instruction mnemonic, the next instruction address, register contents, control line input multiplexer status, the number of microsequencer cycles executed, and the simulated elapsed time are displayed for each instruction executed. Figure 96 indicates that whenever a breakpoint is encountered by the simulator, regardless of whether the trace option is in effect or not, the breakpoint address instruction trace is displayed and the simulator pauses and waits for interaction from the terminal operator.

The long or expanded simulation trace mode (Figure 97) displays all the information returned by the "quick trace" mode and, in addition, displays the original code written for the meta-assembler and the machine language bit pattern output of the meta-assembler. From this expanded trace, errors in programming



EXAMPLE OF SCREEN OUTPUT FROM MICROCODE SIMULATOR WHEN OPERATING IN ITS "QUICK TRACE" MODE.

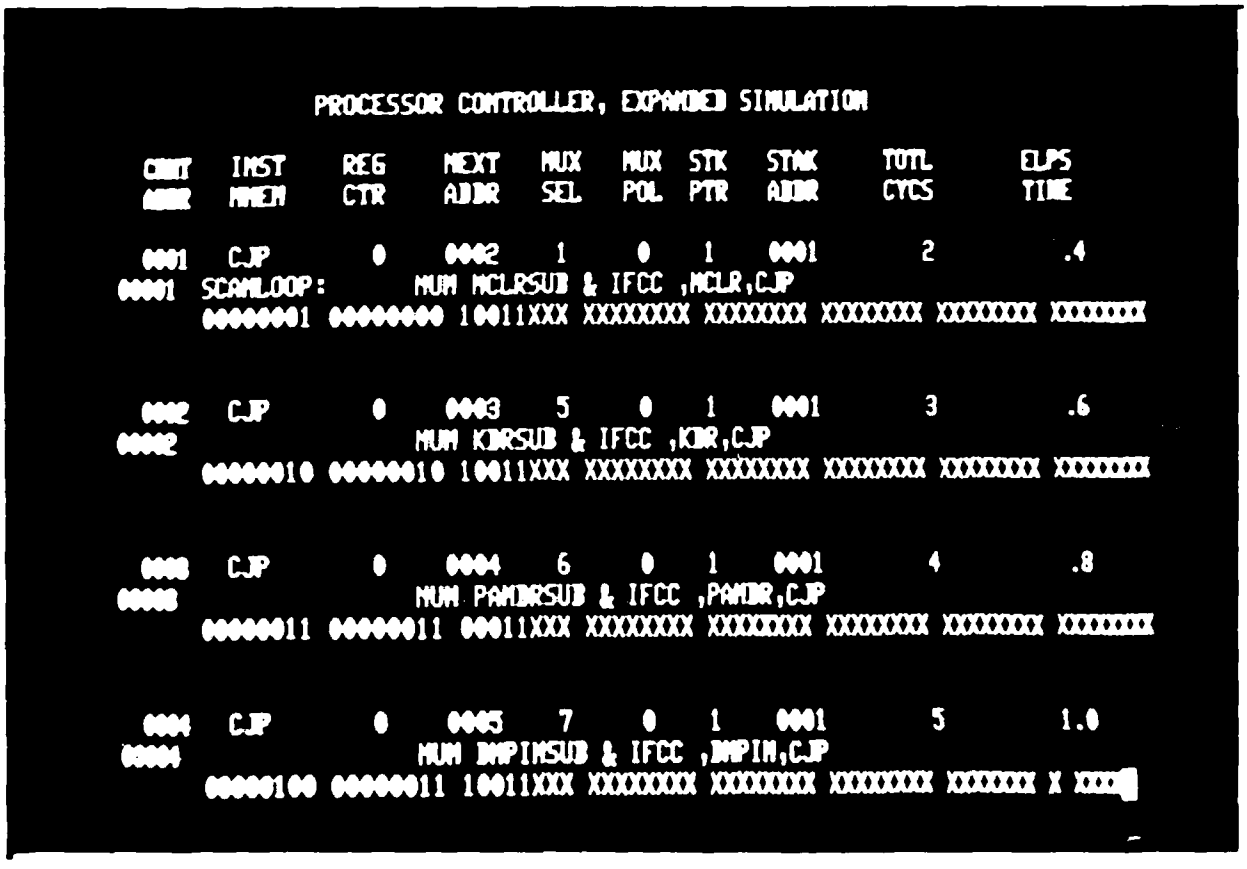
FIGURE 95



```
? 2
 CC POINTER = 2

                MICROSEQUENCER IN QUICK TRACE MODE

 CRNT   INST    REG    NEXT   MUX   MUX  STK  STAK     TOTL      ELPS
 ADDR   MNEM    CTR    ADDR   SEL   POL  PTR  ADDR     CYCS      TIME

 0001   CJP       0    0002    1     0    1   0001        9       1.8
 0002   CJP       0    0003    5     0    1   0001       10       2.0
 0003   CJP       0    0004    6     0    1   0001       11       2.2
 0004   CJP       0    0005    7     0    1   0001       12       2.4
 0005   CJP       0    0060    2     0    1   0001       13       2.6
 0060   CJP       0    0061    9     0    1   0001       14       2.8
 0061   CJP       0    0062   10     0    1   0001       15       3.0

    PROGRAM IS AT BREAK POINT ADDRESS 0061
 0061   CJP       0    0062   10     0    1   0001       15       3.0

 0 = GO TO THE MENU
 1 = CONTINUE
 2 = STOP THE PROGRAM
?
```

EXAMPLE OF SCREEN OUTPUT FROM "QUICK TRACE" VERSION OF MICROCODE SIMULATOR WHEN A BREAKPOINT ADDRESS HAS BEEN REACHED.

FIGURE 96



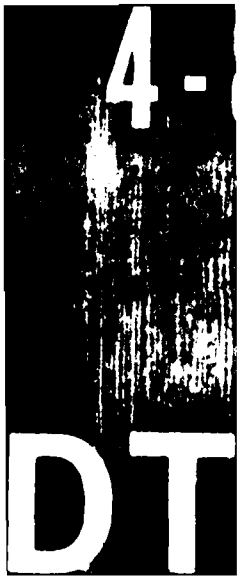
EXAMPLE OF SCREEN OUTPUT FROM "EXPANDED TRACE" VERSION OF MICROCODE SIMULATOR.

FIGURE 97

can more readily be determined without the need to refer back to the original program listing. In the bit pattern information, a "zero" indicates false or inactive control line status, while a "one" indicates a true or active control line status during that particular instruction cycle. An "X" indicates a "don't care" condition, that is, a bit position that was not set by the meta-assembler. All "X's" are eventually converted to zeros by the simulator.

A software effort has been initiated to simulate the instruction set of a much more powerful second generation microprogram sequencer presently in development. Trial sections of code will then be written in both assembly languages. The results of these trials will be used to develop a "best instruction set" for a microsequencer which would be suitable for eventual implementation on a configurable gate array or a macrocell array. Prospects are excellent that the microsequencer can eventually be implemented in Gallium Arsenide (GaAs) technology. Such a microsequencer would be an extremely high-speed supervisor for the programmable control of ultra high-speed arithmetic processors of the future.

*USGPO: 1983 659-062-787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